Targeting Leakage Constraints during ATPG[*]

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Abstract

In previous technology generations IDDQ testing used to be a powerful technique to detect physical faults that are not covered by standard fault models or functional tests. Due to shrinking feature sizes and consequently increasing leakage currents IDDQ testing becomes difficult in the deep-submicron area. One of the problems is the vector dependency of leakage current. Even in good devices the leakage current may vary significantly from one test vector to the next.

In this work we present an ATPG framework that allows to generate test vectors within tight constraints on leakage currents. The target range for the leakage current is automatically determined. Experiments on the ITC99 benchmark suite yield testsets that achieve 100% fault coverage for the larger circuits, even when the range is narrowed down to 50% of the standard deviation of random vectors.

1 Introduction

Measuring the steady state power supply current of a circuit (IDDQ) is a testing technique that is orthogonal to traditional techniques based on fault models or functional tests. Therefore IDDQ testing was helpful in identifying erroneous chips at low testing costs [12]. One of the advantages is that the observation of faults does not depend on voltage levels measured at primary outputs of a circuit. Instead the leakage current of the complete circuit drawn from the energy supply is considered. As a result the observability increases drastically. Previous studies have shown that IDDQ testing identifies a large range of failures some of which are covered – and even more important – some of which are not covered by standard fault models such as stuck-at and path delay [10]. Even failures not detected by functional tests can be identified using IDDQ testing [10].

Unfortunately, the leakage current is not constant but depends on process variations and on the test vectors. Due to process variations the leakage current of two chips may be different even for the same test vector. Here, only statistical methods can be applied to seperate systematic fluctuations due to the location on the wafer, random fluctuations, and fault effects [13]. Models for test vector dependencies of leakage currents are known [1], but usually not applied during IDDQ testing. Both types of variation increase with shrinking feature sizes. Thus process variations or test vector dependencies may hide fault effects, making it harder to differentiate good and bad devices.

Several methods for postprocessing measured leakage data are available to remove variations. Current signatures [7] are created by sorting the measured leakage currents by increasing values. This sorting process reduces the difference in leakage currents from one point to the next. Thus, a fault causes a jump in the signature which helps to identify unexpected behavior more easily. By this the differentiation of good devices from bad devices improves. Other techniques [14], e.g. delta IDDQ [17], have been proposed as an improvement over current signatures. Here the difference of the IDDQ values for different chips or different test vectors is used. However, all of these methods are applied after measuring IDDQ while the significant increase in leakage currents strengthens the inlfuence of vector dependencies. Thus, discontinuities occur even for good devices after sorting.

Tools for *Automatic Test Pattern Generation* (ATPG) have been proposed to generate test vectors for IDDQ testing. These approaches mainly address issues of fault extraction and fault modeling [9]. Once the faults are modeled only constraints due to the logic function of the circuit are considered during ATPG [9, 2, 8, 12]. As a result the leakage current may vary significantly from one test vector to the next due to the dependency of the leakage current on the internal state of a circuit.

Therefore this work suggests to take leakage constraints already during ATPG into account. This reduces the vector dependencies of IDDQ measurements. The above mentioned techniques [7, 17, 13] are orthogonal and can still be applied. An ATPG framework to generate test vectors within a predefined range of leakage currents is presented. This target range is determined by estimating a distribution of the leakage current with respect to test vectors based on random simulation. Then the ATPG framework is guaranteed to generate test vectors only within this target range. The single pseudo stuck-at fault model is considered for combinational ATPG. Deterministic pattern generation, random pattern generation and fault simulation are applied as in standard ATPG frameworks. Additionally, the expected leakage current is calculated for each test vector

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to guarantee that test vectors do not violate the leakage constraints. Experimental results show that the fault coverage does not decrease for the larger ITC99 benchmark circuits in a 90nm technology. At the same time discontinuities are removed from the current signatures that become nearly linear with a small slope. Compared to ATPG without constraints the range of the leakage currents of test vectors shrinks by up to 93 %. This supports discriminating good and bad devices based on IDDQ measurement.

The paper is structured as follows: The model used for leakage calculations and the automatic derivation of a target range for leakage currents adjusted to the circuit under test are introduced in Section 2. The ATPG framework and its components are presented in Section 3. Section 4 provides experimental results. Conclusions and future work are discussed in Section 5.

2 Leakage Constraints

In the following the leakage model used in this work is introduced. Based on this model the automatic derivation of the leakage constraints for ATPG is briefly discussed.

2.1 Leakage Model

The main component of the leakage current in a digital circuit is given by the sum of the sub-threshold leakages of the transistors [1]. Therefore, the leakage current of a single gate g depends on the values assigned to the input signals of the gate, i.e. the state of the gate. Given a library of gates and process parameters, the leakage current l_g of a gate g is given by a mapping of the type t^g of the gate and the values $x_1^g, \dots x_n^g$ of the gate inputs of the gate to the leakage current:

$$l_g : \{t^g, x_1^g, \dots, x_n^g\} \to v$$

Then, the leakage current L_C for a given circuit C under a certain assignment $i_1, \dots i_m$ to the primary inputs is the sum of the leakage currents of all gates, where the state of a gate depends on the assignment to the primary inputs:

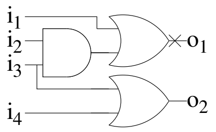
$$L_C = \sum_{g \in C} l_g(t^g, x_1^g(i_1, \dots i_m), \dots x_n^g(i_1, \dots i_m)$$

In the following only complete assignments to the primary inputs are considered when estimating the leakage currents. Therefore the leakage current of a gate does not have to be described as a function of the primary inputs of the circuit. Instead the input assignment is simulated, afterwards each gate is in a defined state and the corresponding leakage values are added.

Integer arithmetic is applied during this process. Given a gate library that specifies the leakage currents, the leakage values for all gates are multiplied by the same factor; then the values are rounded to the next integer value and divided by their greatest common divisor. Moreover, our implementation uses an event based simulator to efficiently update the leakage values for test vectors.

state	AND	OR
0 0	8pA	16pA
0 1	11pA	13pA
1 0	13pA	11pA
1 1	16pA	9pA

Real data is confidential; the table reflects the ratios of a real library (180nm, 1.8V).
(a) Currents



(b) Circuit

Figure 1. Vector dependencies

Example 1 *Figure 1(a) exemplary shows the leakage currents for 2-input AND and OR gates. The leakage current depends on the state of the inputs. Now considering the circuit in Figure 1(b) yields a leakage current of* $13+16+11 = 40$ *pA for the assignment* $\{i_1 = 0, i_2 = 1, i_3 = 1, i_4 = 0\}$. *The assignment* $\{i_1 = 1, i_2 = 0, i_3 = 0, i_4 = 1\}$ *causes a leakage current of* $11 + 8 + 13 = 32$ *pA.*

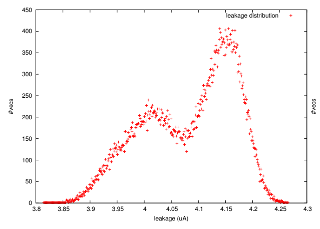
2.2 Target Range

The objective of this work is to create test vectors within a small range of leakage currents to minimize the variations due to vector dependencies. This decrease improves the resolution of post processing the data using current signatures [7] or delta IDDQ [17]. Of course, a suitable range depends on the circuit under consideration. Figure 2 shows histograms of leakage currents for the circuits *b12* and *b19* of the ITC99 benchmark suite. These results were obtained from leakage calculations for 64000 random vectors using a 90nm process library. Vectors with similar current values were grouped. The x-axis gives the leakage current, while the y-axis shows the number of vectors in each group. Circuit *b12* exhibits a quite irregular behavior with a large number of different leakage paths that are activated by different sets of test vectors. In contrast *b19* shows a very regular behavior – random simulation leads to a Gaussian distribution of leakage values. Such a “good” behavior was observed for most of the ITC99 benchmarks. In this case most of the input vectors are contained in a small range defined by the mean leakage value μ and the standard deviation σ determined from the random vectors.

Therefore the interval $[\mu - \alpha\sigma, \mu + \alpha\sigma]$ is used to define the range targeted during test vector generation, where α is a small user-defined value. Choosing α too large does not restrict test pattern generation, the variation in leakage current between test vectors is not reduced. Choosing α too small restricts test pattern generation too much. As a result the run time for test pattern generation increases, because finding a vector within the specified range is hard. Also the number of faults that do not have a test vector in the specified range increases.

3 ATPG Framework

In the following the ATPG framework is described to generate test vectors under leakage constraints. First, the underlying fault model and an introductory example are given, then the framework is described.


(a) For b12

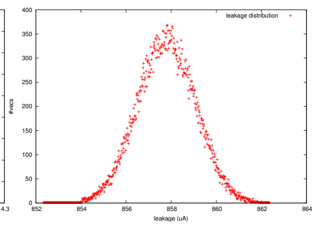

(b) For b19

Figure 2. Leakage distributions (90nm)

3.1 Fault Model

One fault model typically considered to generate test vectors for IDDQ testing is the single *Pseudo Stuck-At Fault* (PSF) model [11, 12]. Similar to the well-known *Stuck-at Fault* (SF) model a fault fixes a line to a constant value. The fault is detected by an input assignment that forces the signal to the fault free value. In case of an SF the fault can only be observed at primary outputs. In contrast, a PSF is observed indirectly by measuring the leakage current. Therefore propagation to primary outputs is not necessary. For this reason test pattern generation for PSFs is computationally less intensive than for SFs. Also any single test vector already detects half of the PSFs in any circuit.

Besides the PSF model, bridging faults are often considered for IDDQ testing [11, 12]. The extension of the framework proposed here to handle bridging faults is straight forward and therefore not considered in more detail.

The survey in [8] provides an overview of additional fault models and fault extraction techniques used in IDDQ testing.

3.2 Introductory Example

The following example shows that leakage currents may vary significantly within the potential test vectors even for a single fault. This observation is the foundation for the ATPG framework presented afterwards.

Example 2 *Recall the circuit discussed in Example 1. Assume the PSF-0 is to be tested at output o_1. A test vector is a partial assignment to the inputs that sets o_1 to 1, e.g. $t_1 = \{i_1 = 0, i_2 = 1, i_3 = 1\}$. Setting i_4 to 0 causes a total leakage current of* 40 *pA, while setting i_4 to* 1 *causes a leakage current of* 38 *pA. An alternative test vector for the same fault is $t_2 = \{i_1 = 1, i_2 = 0, i_3 = 0\}$. Under $i_4 = 1$ this vector yields a leakage current of only* 32*pA.*

3.3 Main Flow

The main flow for test pattern generation is shown in Figure 3. In step (A) the target range is determined. As described in Section 2.2 random simulation is carried out for a user defined number l^R of vectors to estimate the values μ and σ. The user defined parameter α fixes the target range for the subsequent test pattern generation steps. These steps consist of alternating random pattern generation and deterministic pattern generation similar to standard ATPG flows.

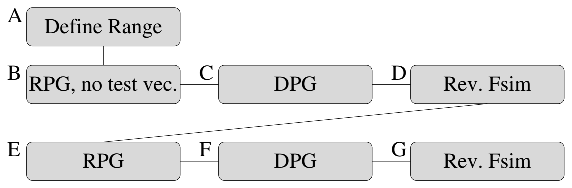


Figure 3. Overall ATPG flow

First *Random Pattern Generation* (*RPG*) (B) is carried out to remove faults that can easily be detected by random vectors. During this step no test vectors are collected. Fault simulation is only done for vectors within the predefined leakage range. Detected faults are not considered in the following *Deterministic Pattern Generation* (DPG) step (C). The next section explains this step in detail. During the DPG step test vectors within the leakage range are collected in the testset. Also faults untestable due to logic constraints – not due to leakage constraints – are classified in this step. Then, all except untestable faults are considered for reverse fault simulation of the test vectors collected so far (step (D)): Fault simulation for all test vectors collected so far is done in reverse order; vectors that do not detect additional faults are discarded. Moreover, typically some faults are not detected by these test vectors, therefore a second RPG is done in step (E). This time valid test vectors that detect at least one additional fault are collected. Remaining faults are considered in the final DPG step (F). Then reverse fault simulation is applied to the testset again (step G) to reduce the size.

Alternatively, even more elaborate configurations of RPG, DPG and fault simulation are possible. Here, we use this simple environment, to evaluate efficiency and fault coverage that can be achieved by the proposed method.

3.4 Deterministic Pattern Generation

Figure 4 describes the two DPG steps within the main flow in more detail. This procedure is applied to each fault that is passed to the DPG step. First an engine for deterministic test pattern generation is called (step (1)) to decide whether the fault is untestable (step (2)). In this case the next fault is considered.

Alternatively, the DPG engine generates a test vector. The test vector is typically only a partial assignment to the primary inputs. To accurately determine the leakage, the test vector is randomly extended to a full assignment (step (3)). Next, the leakage current is determine for this test vector (step (4)). If the leakage current is within the target range, the (fully assigned) test vector is stored (step (5)), fault simulation (step (6)) is done to classify other faults detected by the same test vector and the fault is marked testable (step (7)).

If the first random extension of the test vector did not yield an input vector within the specified leakage range, random extension (step (3)) and leakage estimation (step (4)) are repeated until either a valid test vector has been found or a given limit l^R is reached.

If the limit l^R is reached without finding a valid test vector, the DPG engine is called again (step (8)) to retrieve

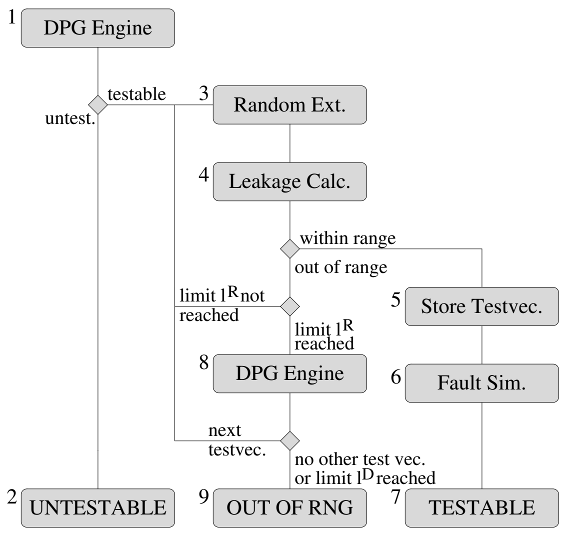


Figure 4. DPG step with leakage constraints

a new test vector. If a new test vector exists, the random extension process is repeated. Otherwise, if no other test vector exists or a second predefined limit l^D for the number of test vectors is reached, the process terminates. The current fault is classified as being "out of range" (step (9)).

As a DPG engine any algorithm is suitable that allows to explore all test vectors for a given fault. Here, a DPG engine based on *Boolean Satisfiability* (SAT) similar to [16, 4] is used. The Minisat solver [5] is the underlying reasoning engine. In this case "blocking clauses" are inserted into the search problem to find new test vectors. A blocking clause can be derived directly from a test vector.

Using random extension to decide whether there exists a test vector for a given fault is a heuristic procedure. Finding better heuristics for this step is future work. Due to the heuristic procedure faults may be classified as being out of range, even if a test vector exists. But as an advantage the problem size that has to be handled by the DPG engine is restricted to the fanin cone of the fault site. Moreover, the leakage model only has to be handled outside the DPG engine and no tight integration is necessary. This leads to a "lazy approach", i.e. the decision whether a test vector is valid is only done after evaluating the functional constraints.

Alternatively, an "eager approach" can be used. In this case the leakage model is tightly integrated with the formal procedure for test pattern generation. Similar procedures integrating Boolean reasoning and leakage estimation have been proposed to find input vectors with minimal leakage current [3, 6, 15]. These procedures are based on frameworks to solve satisfiability of pseudo Boolean constraints or 0-1 integer linear programs. But handling the leakage model within the formal reasoning engine is quite resource intensive – even deriving a single vector with minimal leakage takes a long run time and may not even be possible for all circuits. In the ATPG framework considered here a large number of faults is considered and therefore a larger number of test vectors may have to be generated. Thus using an "eager approach" is not feasible in this context. Nonetheless, using a fully deterministic procedure in the rare case where the heuristic approach fails to generate a test vector for a particular fault, is an interesting future extension to the framework presented here.

4 Experimental Results

In this section the framework is evaluated using benchmark circuits. First, the dependence between run time, fault coverage and size of the testset on the leakage constraints is studied. Then, the practical benefit for IDDQ testing is assessed by considering the leakage signatures of the testsets for different α.

Circuits of the ITC99 benchmark suite are used to evaluate the proposed framework. A library for a 90nm feature size that consists of 2-input gates has been used. Gates with more inputs were decomposed into 2-input gates for the experiments. The PSF model is considered for test pattern generation. All experiments were carried out on an Intel Core Duo 2 (4MB Cache, 4 GB RAM, 3 GHz, Linux). The parameter l^R determines the number of random vectors used to estimate μ and σ and the number of random extension to a deterministic test vector (see Section 3.3 and Section 3.4). This parameter was manually adjusted to the size of the circuit and ranges from 40 (for the small circuits *b01*, *b02*, *b03*, and *b06*) to 20,000 (for the large circuits *b18* and *b19*)[1]. The parameter l^D limits the number of (typically partial) deterministic test vectors that are considered for random extensions (see Section 3.4) and was set to 100 for all circuits. Prior to test pattern generation fault collapsing was applied to reduce the number of target faults.

Table 1 shows results for different values of the parameter α for some ITC99 benchmarks; the case $\alpha = \infty$ describes standard ATPG. The same framework was used for standard ATPG, but the leakage estimation was deactivated. The run times required for the different tasks are shown in column *time*. The total time *tot* includes that for *DPG*, *RPG* and reverse fault simulation (*rev*). During DPG, RPG, to define the targeted leakage range and to sort the test vectors the leakage current was calculated. The cumulative time is given in column *leak*. The number of test vectors in the testset is given in column *#tv*. Column *#oor* (out of range) gives the number of faults that are testable without leakage constraints, but have no test vector in the generated testset. This is also reflected by the fault efficiency in column *%fe*, i.e. the percentage of testable faults detected by the testset.

The smaller the value of α the tighter is the target range for leakage currents and the harder is test pattern generation. Thus, run times increase when the range narrows. The dominating factor is the time needed for leakage calculations during random as well as deterministic test pattern generation. In particular, when no test patterns are found for many faults, the run time increases significantly (e.g. *b15_1*). For other circuits the increase in run time is not too large. All ITC99 circuits were completely handled by the framework.

The testset should be as small as possible since the size is proportional to the time needed to test a circuit. Using leak-

[1]Fault simulation for a large number of random vectors was done. Then, l^R was choosen where the number of newly detected faults using additional vectors became small. Automating this step remains future work.

age constraints, the testset only increases marginally and may even be smaller in some cases, e.g. consider *b15* or *b19* for $alpha = 0.5$. Moreover, the number of faults that could not be classified within tight ranges for the leakage estimation is small. For the very small circuit *b06*, the number of faults that remain undetected by vectors within the target range is large compared to the total number of faults. Testing a fault in a small circuit typically forces values on most of the primary inputs, therefore "adjusting" the leakage current by extending the test vector is difficult. In contrast, for the larger circuits, typically all faults were classified even for the smallest values of α. A fault efficiency of 100% is achieved for the benchmark circuits *b18* through *b22*.

In practice a post processing step after measuring leakage currents is applied to reduce the influence of process variations that may cause an offset and to reduce the expected variations due to vector dependencies. One technique is to sort the test vectors by their leakage current prior to deciding whether the leakage measurement unveils an unexpected behavior of some device [7]. Therefore such a sorting process is applied here and the resulting leakage signatures are compared to standard ATPG. The plots in Figure 5 show the results. Again, different values for α are considered, $\alpha = \infty$ denotes the results obtained without restrictions on leakage currents.

Without any restrictions the leakage current from one vector to the next is quite unstable even after sorting. The signature typically shows a large slope and also significant fluctuations may occur from one test vector to the next.

For *b12* the curve remains unstable for $\alpha \geq 2$. When tightening the interval by reducing α, large jumps are not contained in the signature any more. The signature converges to linear with a small slope. For the circuits *b14* to *b22* the range of expected currents was reduced to 19% or less for $\alpha = .5$ compared to $\alpha = \infty$. In case of *b17_1* a reduction to 9% was achieved.

Expecting such a continuous signature for good devices helps in practice. Erroneous devices that deviate from this behavior are identified much easier compared to a discontinuous signature with a large slope.

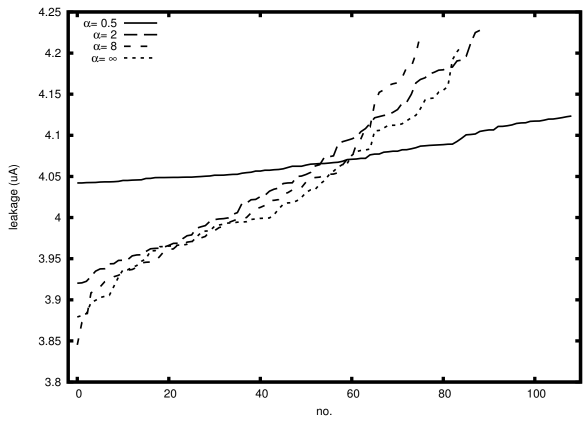
5 Conclusions

This paper proposed a framework for leakage aware ATPG. Using test vectors generated by this framework implies a high practical benefit during IDDQ testing. The ITC99 benchmark suite was used to evaluate the framework. As the most important result quite continuous leakage signatures with a small slope were retrieved for the generated testset. This "pre-measurement" approach can directly be combined with post-processing techniques like e.g. [7, 17, 13].

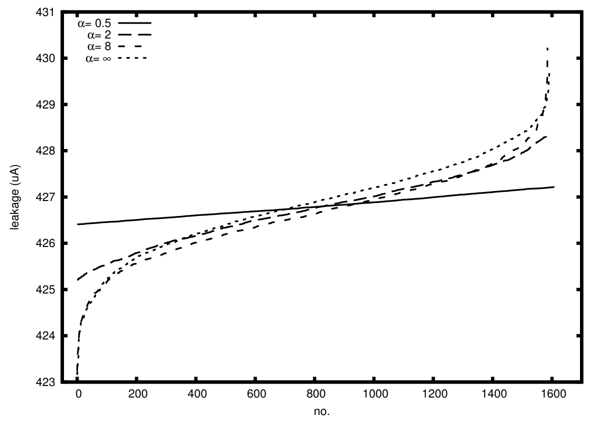
Using the framework comes at a penalty in run time for generating test vectors. Therefore improving the estimation of leakage current is a major goal for future work. Including a deterministic reasoning engine that considers the leakage model to further increase the fault coverage and including the bridging fault model are other topics for future work. For technologies below 90nm leakage currents tend to increase due to decreasing feature size. Thus, an even more beneficial impact is expected.

Table 1. Results for different values of α

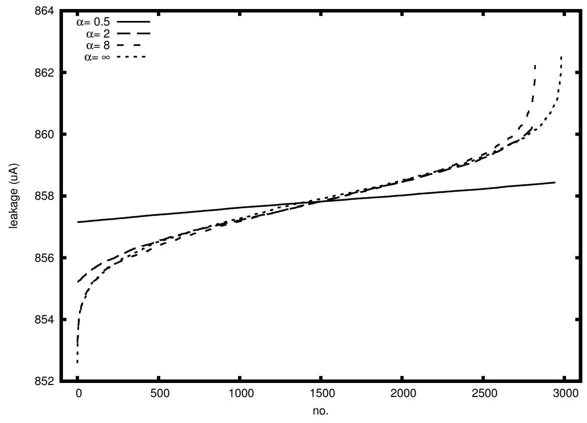
circ	α	time					#tv	#oor	%fe
		tot	DPG	RPG	rev	leak			
b06	0.5	<0.0	<0.0	<0.0	<0.0	<0.0	5	10	92.1
	2	<0.0	<0.0	<0.0	<0.0	<0.0	7	0	100.0
	8	<0.0	<0.0	<0.0	<0.0	<0.0	8	0	100.0
	∞	0.0	<0.0	<0.0	0.0	0	7	0	100.0
b12	0.5	0.6	0.1	0.3	0.0	0.5	110	0	100.0
	2	0.5	0.0	0.3	<0.0	0.4	89	0	100.0
	8	0.3	<0.0	0.2	0.0	0.3	76	0	100.0
	∞	0.0	0.0	0.0	<0.0	0	85	0	100.0
b13	0.5	0.1	0.0	0.0	<0.0	0.1	23	0	100.0
	2	0.1	<0.0	0.1	<0.0	0.1	21	0	100.0
	8	0.1	<0.0	0.1	<0.0	0.1	20	0	100.0
	∞	0.0	<0.0	0.0	<0.0	0	21	0	100.0
b15	0.5	1431.6	1392.8	25.4	0.9	1428.7	285	1	100.0
	2	43.9	7.4	24.0	0.7	42.4	276	0	100.0
	8	31.6	0.4	20.5	0.6	30.6	294	0	100.0
	∞	3.0	1.0	1.0	0.9	0	288	0	100.0
b15_1	0.5	29036.1	28977.4	38.4	2.0	29025.8	363	800	96.8
	2	16026.7	15971	36.8	1.6	16018.8	390	556	97.8
	8	50.0	0.5	32.7	1.3	47.4	375	0	100.0
	∞	5.8	1.4	2.4	1.9	0	363	0	100.0
b17	0.5	7886.0	7654.8	148.0	9.9	7872.0	735	36	99.9
	2	245.6	23.9	143.3	8.4	232.4	734	0	100.0
	8	215.3	3.5	137.2	7.9	202.5	749	0	100.0
	∞	36.8	7.3	18.4	10.7	0	730	0	100.0
b17_1	0.5	65151	64886.6	167.9	14.3	65127.4	909	378	99.5
	2	324.7	69.4	163.5	12.8	304.6	910	0	100.0
	8	251.9	5.3	158.7	11.7	233.0	929	0	100.0
	∞	48.7	9.8	21.7	16.6	0	903	0	100.0
b18	0.5	1764.4	147.7	1036.9	67.5	1681.1	1614	0	100.0
	2	1623.6	31.3	1028.7	61.3	1535.2	1596	0	100.0
	8	1594.1	26.4	1014.7	58.0	1509.6	1587	0	100.0
	∞	262.6	47	134.5	79.5	0	1594	0	100.0
b18_1	0.5	1652.9	152.7	961.1	64.9	1572.5	1640	0	100.0
	2	1507.5	30.2	954.9	57.4	1423.7	1604	0	100.0
	8	1483.7	25.9	943.7	56.0	1399.8	1608	0	100.0
	∞	246.9	43.7	126.6	75.2	0	1589	0	100.0
b19	0.5	3835.6	425.6	2112.4	251.8	3549.2	2950	0	100.0
	2	3495.9	125.1	2114.2	223.7	3212.5	2828	0	100.0
	8	3464.6	119.6	2099.5	220.7	3183.9	2823	0	100.0
	∞	732.0	169.4	265.6	293.5	0	2982	0	100.0
b19_1	0.5	3574.5	395.7	1964.5	242.7	3296.6	2966	0	100.0
	2	3262.0	120.2	1967.5	213.8	2990.6	2841	0	100.0
	8	3239.6	113.9	1959.7	212.5	2966.3	2834	0	100.0
	∞	691.6	159.2	256.3	272.8	0	2874	0	100.0
b20	0.5	76.8	19.6	37.2	1.2	75.1	144	0	100.0
	2	54.5	0.4	35.2	1.0	53.1	155	0	100.0
	8	51.3	0.4	33.3	0.9	49.9	156	0	100.0
	∞	5.1	0.8	2.9	1.2	0	124	0	100.0
b20_1	0.5	41.4	1.3	26.0	0.8	40.3	142	0	100.0
	2	37.9	0.2	24.5	0.7	36.9	136	0	100.0
	8	35.6	0.2	23.0	0.6	34.6	135	0	100.0
	∞	3.2	0.6	1.6	0.8	0	112	0	100.0
b21	0.5	145.4	68.5	50.1	1.3	143.5	169	0	100.0
	2	73.6	0.6	47.7	1.2	71.9	174	0	100.0
	8	68.9	0.4	44.9	1.0	67.3	167	0	100.0
	∞	6.4	0.9	4.0	1.3	0	141	0	100.0
b21_1	0.5	53.9	1.3	34.4	0.8	52.8	147	0	100.0
	2	49.8	0.4	32.4	0.7	48.7	154	0	100.0
	8	46.5	0.3	30.4	0.6	45.6	143	0	100.0
	∞	3.8	0.7	2.1	0.9	0	133	0	100.0
b22	0.5	118.5	4.5	74.2	2.1	115.7	191	0	100.0
	2	109.6	1.0	70.9	2.0	106.7	205	0	100.0
	8	104.0	0.7	67.5	1.8	101.4	203	0	100.0
	∞	11.1	1.7	6.5	2.5	0	176	0	100.0
b22_1	0.5	87.3	3.4	54.6	1.6	85.2	192	0	100.0
	2	79.9	0.7	51.7	1.4	77.9	189	0	100.0
	8	75.4	0.5	48.9	1.2	73.6	181	0	100.0
	∞	7.6	1.1	4.6	1.7	0	157	0	100.0



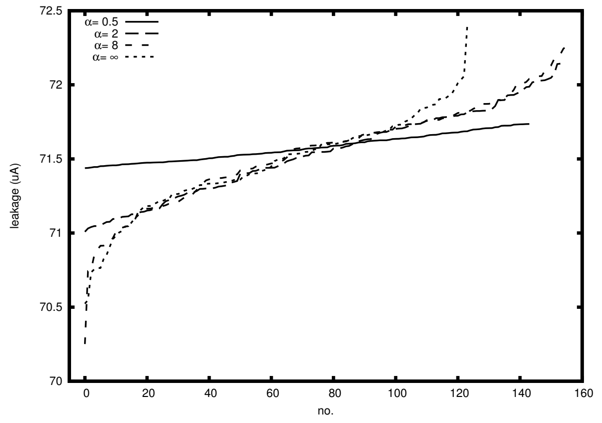
(a) For b12



(b) For b18



(c) For b19



(d) For b20

Figure 5. Signatures of testsets

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