Exploiting Negative Control Lines in the Optimization of Reversible Circuits

Kamalika Datta[1], *Gaurav Rathi*[2], *Robert Wille*[3,4]
Indranil Sengupta[2], *Hafizur Rahaman*[1], *Rolf Drechsler*[3,4]

[1] Department of Information Technology, Bengal Engineering & Science University, Shibpur, Howrah 711103, India
Email: kdatta.iitkgp@gmail.com, rahaman_h@it.becs.ac.in
[2] Department of Computer Science & Engineering, Indian Institute of Technology, Kharagpur 721301, India
Email: gaurav.rathi01@gmail.com, isg@iitkgp.ac.in
[3] Institute of Computer Science, University of Bremen, 28359 Bremen, Germany
Email: {rwille, drechsle}@informatik.uni-bremen.de
[4] Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany

Abstract. The development of approaches for synthesis and optimization of reversible circuits received significant attention in the past. This is partly due to the increasing emphasis on low power design methodologies, and partly motivated by recent works in quantum computation. While most of them relied on a gate library composed of multiple-control Toffoli (MCT) gates with positive control lines, some initial works also exist which additionally incorporate negative control lines. This usually leads to smaller circuits with respect to the number of gates as well as the corresponding quantum costs. However, despite these benefits, negative control lines have hardly been considered in post-synthesis optimization of reversible circuits so far. In this paper, we address this issue. We are presenting an optimization scheme inspired by template matching which explicitly makes use of negative control lines. Experimental evaluations demonstrate that exploiting negative control lines in fact lead to a reduction in the number of gates and the quantum costs by up to 60% and 25%, respectively.

Keywords: Reversible Circuits, Optimization, Negative control gates, Template Matching

1 Introduction

Despite the sustained advancements in semiconductor technology over the last few decades, conventional circuit technologies are approaching severe physical

boundaries particularly caused by the exponential miniaturization. Besides that, engineers are facing consequent demands for the development of ultra-low-power designs. Motivated by this, there has been several attempts by researchers to look for alternative circuit technologies. In the recent past, reversible logic circuits received significant attention as a viable and futuristic technology to address these issues.

For low-power design, reversible logic offers interesting advantages since almost zero power dissipation will only be possible if computation is reversible [1, 2]. Also in the domain of low-power on-chip interconnect encoding promising solutions can be achieved when exploiting reversible computations [3]. Besides that, research on reversible circuits has been further strengthened by recent accomplishments in the domain of quantum computation [4], since the basic quantum operations are reversible in nature.

Consequently, the development of approaches for synthesis and optimization of reversible circuits received significant attention in the past (see e.g. [5–8]). The problem is thereby significantly different from that of conventional logic circuits – in particular, since established concepts such as fan-out and feedback are not directly allowed in reversible circuits [4]. Because of the complexity of the problem, most of the approaches generate sub-optimal netlists of reversible gates. Hence, there is an ample scope for post-synthesis optimization.

Approaches addressing this issue have already been introduced. More precisely, techniques such as template matching [9] or window optimization [10] have been presented. But they relied on a gate library composed of multiple-control Toffoli (MCT) gates with positive control lines. Instead, additionally considering negative control lines often leads to reductions in the number of gates and quantum cost. However, while the functional power of negative control lines has already been exploited in synthesis, this has hardly been considered in post-synthesis optimization of reversible circuits so far.

In this paper, we address this issue. We are presenting an optimization scheme inspired by template matching which explicitly makes use of negative control lines. That is, so-called templates (generalized to rules) are introduced that allow for a substitution of a cascade of (positively controlled) Toffoli gates with a single but functional equivalent (negatively controlled) Toffoli gate. Rules for both, positive and negative controlled Toffoli gates, have thereby been proposed. Experimental evaluations demonstrate that exploiting negative control lines in fact leads to a reduction in the number of gates and the quantum costs by up to 60% and 25%, respectively.

The rest of the paper is organized as follows. Section 2 gives a brief introduction to reversible circuits followed by the general motivation of the work in Section 3. The proposed optimization approach is discussed in Section 4. Section 5 presents and discusses the obtained results followed by conclusions in Section 6.

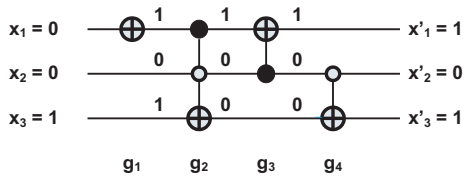


Fig. 1. Reversible Circuit

2 Reversible Functions and Circuits

A Boolean function $f : \mathbb{B}^n \to \mathbb{B}^n$ is *reversible* if it is bijective, i.e. if each input pattern is uniquely mapped to a corresponding output pattern. The *synthesis problem* is defined as the task of determining a reversible circuit for a given function f.

Reversible circuits differ from conventional circuits, since e.g. fanout and feedback are not directly allowed [4]. Usually, they are built as a cascade of reversible gates, like the Toffoli gate [11] or the Fredkin gate [12]. In this paper, we focus on circuits composed of multiple-control Toffoli (MCT) gates.

Definition 1. *Let $X = \{x_1, \ldots, x_n\}$ be a set of variables or lines. Then, a reversible circuit is described as a cascade $g_1 \ldots g_d$. A* multiple control Toffoli *(MCT) gate $g_i = (C_i, t_i)$, $i \in \{1, \ldots, d\}$, is a tuple of a set $C_i \subset \{x^\varrho \mid x \in X, \varrho \in \{-, +\}\}$ of (positive and negative)* control lines *and a* target line *$t_i \in X$ with $\{t_i^-, t_i^+\} \cap C_i = \emptyset$. The target line t_i of a Toffoli gate is inverted if and only if all positive (negative) control lines evaluate to one (zero). The values of all remaining lines are passed through the gate unaltered. That is, the Toffoli gate maps $(x_1, \ldots, x_{t_i}, \ldots, x_r)$ to $(x_1, \ldots, \bigwedge_{x \in C_i} \dot{x} \oplus x_{t_i}, \ldots, x_r)$ with $\dot{x} = x$ for any x^+ and $\dot{x} = \overline{x}$ for any x^-.*

Example 1. Fig. 1 shows a reversible circuit with three lines and composed of four gates. The target lines are denoted by $\oplus$, while a $\bullet$ represents a positive control line and a $\circ$ represents a negative control line. For example, assigning the input pattern 001 to the circuit results in the output pattern 101. Due to the reversibility, this computation can be performed in both directions.

In order to evaluate the *costs* of a reversible circuit, the following two metrics are applied:

- The *gate count* (GC) denotes the number of MCT gates in the final netlist.
- The *quantum costs* (QC) denote the effort needed to transform a reversible circuit to a quantum circuit based on the principles proposed in [13]. For positively controlled Toffoli gates, we apply thereby the metric as used in *RevKit* [14]. If negative control lines occur, the same cost metric is applied except for the case where the Toffoli gate is entirely composed of negative controls. In this special case, the costs are increased by one for this particular gate [15].

Table 1. All 3-input negative and positive gate realizations

Toffoli gate			Equivalent netlist		
Netlist	GC	QC	Netlist	GC	QC
	1	6		4	8
	1	6		4	8
	1	6		4	8
	1	5		2	6
	1	5		2	6
	1	5		2	6
	1	5		2	6
	1	5		2	6
	1	5		2	6
	1	2		2	2
	1	2		2	2
	1	2		2	2
	1	2		2	2
	1	2		2	2
	1	2		2	2

3 Motivation and General Idea

Synthesis and optimization of reversible circuits received significant attention in the past. For this purpose, various approaches have been introduced (see e.g. [5–8]). The majority of them relied thereby on a gate library exclusively composed of MCT gates with positive control lines only. However, if negative control lines are additionally considered, significant reductions with respect to the number of gates as well as the resulting quantum costs can be achieved.

As an example, consider Table 1 showing the pictorial representation of all the possible 3-input Toffoli gates with negative-control lines together with the corresponding *minimal* realizations composed of (positively controlled) Toffoli gates only[5]. Columns denoted by *GC* and *QC* provide the number of gates and quantum costs, respectively. The table clearly shows that a consideration of negative control lines allows for a significantly more compact realization of reversible functionality with respect to both, number of gates and quantum costs.

However, despite these benefits, the exploitation of negative control lines for circuit optimization has hardly been considered yet. Although synthesis and optimization approaches which create circuits composed of negatively controlled Toffoli gates already exist (e.g. ESOP-based synthesis [16–18] or QMDD-based

[5] Note that the minimal realizations have been obtained using the exact synthesis methods proposed in [7].

synthesis [19]), they often just exploited the structure of the respective function representation. More precisely, in ESOP-based synthesis, negative control lines are just applied as they allow for a straight-forward realization of negative literals. In QMDD-based synthesis, negative control lines have been utilized in order to address negatively controlled paths in the data-structure.

Just recently, first approaches have been presented that directly considered negative control lines in order to obtain more efficient circuit realizations. For example, in [20] an exact synthesis approach was proposed that enabled the determination of minimal realizations for small functions. In [21], a group theory-based synthesis approach has been proposed that uses both, negative and positive control lines for synthesis. The results show that, compared to previous approaches, significant reductions in gate count and quantum costs can be achieved directly at the synthesis level.

In this work, we propose an alternative approach that addresses the post-synthesis stage. That is, an optimization approach is presented that explicitly aims for a reduction in the number of gates and the quantum costs of reversible circuits by exploiting the functional power of negative control lines. The general idea for our rules is motivated by Table 1. A careful analysis of the depicted cascades unveils that certainly structured cascades of positively controlled Toffoli gates often subsume into a single negatively controlled Toffoli gate. For example, a cascade of Toffoli gates with all possible combinations of positive control connections can be subsumed into a single Toffoli gate with negative control lines only (see first row in Table 1). Similar observations can be made for the remaining cases in Table 1. By analyzing these patterns, we have formulated *generalized* rules which can be applied in order to reduce the number of gates and the quantum costs for given circuit realizations. In the next section, these rules as well as the resulting optimization approach are described in detail.

4 Proposed Optimization Approach

In this section, we present an approach for optimizing a given MCT gate netlist using certain rules consisting of both positive and negative control lines. As mentioned above, the design of the rules is motivated by an analysis of all possible 3-input negative control gates and the corresponding minimum realizations with positive control gates (see again Table 1). In the following, first the derived rules are presented before the resulting optimization algorithm is sketched and briefly discussed.

4.1 Proposed Templates and Rules

Table 2 presents the proposed rules in terms of the templates together with the equivalent minimal netlists that can be used to replace them. Rules can be applied to cascades of Toffoli gates composed of a different number of lines as denoted in Column n, with certain target line connections as denoted in Column *Targ.L.*, and a total size of gates as denoted on Column *GC* (for gate

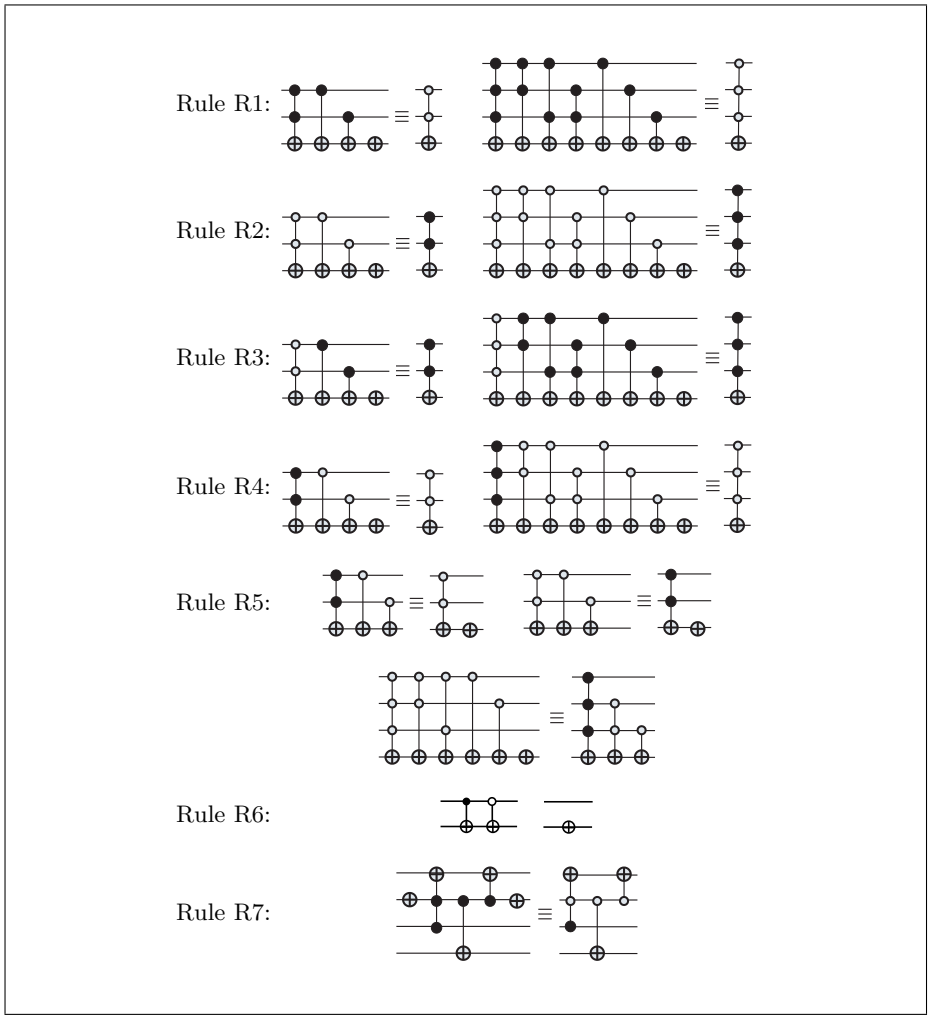
Table 2. The generalized templates and their rules for application

	Template Specification				Replace Template by
	n	$Targ.L.$	GC	Requirement	
R1	k	All on line x	2^{k-1}	Positive control dots appear in all 2^{k-1} possible ways, in lines other than x	One k-input MCT gate, with target on line x, and negative controls on all other lines
R2	k	All on line x	2^{k-1}	Negative control dots appear in all 2^{k-1} possible ways, in lines other than x	One k-input MCT gate, with target on line x, and positive controls on all other lines
R3	k	All on line x	2^{k-1}	One gate with all negative control dots, and other gates having all other possible combinations of positive control dots, in lines other than x	One k-input MCT gate, with target on line x, and positive controls on all other lines
R4	k	All on line x	2^{k-1}	One gate with all positive control dots, and other gates having all other possible combinations of negative control dots, in lines other than x	One k-input MCT gate, with target on line x, and negative controls on all other lines
R5	k	All on line x	$r < 2^{k-1}$	Unique combinations of the control dots appear in the gates (*as per rules R1, R2, R3, R4*)	One k-input MCT gate with all positive (or negative) controls, and the remaining $(2^{k-1} - r)$ MCT gates with the missing unique patterns of control dots
R6	2	All on line x	2	One CNOT gate with negative control dot and one CNOT gate with positive control dot	One NOT gate on line x
R7	k	No restriction	No restriction	Two NOT gates on a line y, with no target placed on line y in any of the gates in between	Remove the NOT gates and complement the polarities of all control dots on line y between the two NOT gates

count). Besides that, the additional requirements as denoted in Column *Requirement* must hold. If all these conditions are satisfied, the considered cascade can be replaced by a more efficient alternative as described in Column *Replace Template by*. Examples illustrating the application of these rules are provided in Table 3.

More precisely, the templates corresponding to rules R1 and R2 can be applied to any cascade composed of 2^{k-1} k-input gates, where all possible combinations of (positive/negative) control line patterns are present. Rules R3 and R4 can be considered as extensions to rules R1 and R2, respectively, where the gate with all control dots has reverse dot polarity as compared to the other gates in the template. For cases in which not an exact but a partial match of the rules

Table 3. Example application of the rules



R1, R2, R3 or R4 can be determined, rule R5 can be applied (as long as this leads to a reduction in the quantum cost). Rule R6 is a simple rule where two CNOT gates of opposite control polarities are combined into a single NOT gate. Rule R7 can be applied to reduce NOT gates in any MCT gate netlist.

The rules are general and, except for R6, can be applied to cascades of MCT gates with an arbitrary number k number of lines.

Algorithm 1: *Template Matching Algorithm*

Input: Cascade of MCT gates $G = \{g_1, g_2, \ldots, g_p\}$
Output: Optimized cascade of MCT gates
begin
  $ngates = p$;
  while (there is change in G) **do**
    begin
      $index = 1$;
      while ($index \leq ngates$) **do**
        begin
          $G_{seg} = find\_seg(G, index)$;
          $apply\_rule(G_{seg})$; // *Using gate swapping, if required*
          $index = index + |G_{seg}|$;
          $ngates = compact\_netlist(G)$;
        end
    end
end

4.2 Algorithm

Using the rules introduced above, the proposed optimization approach traverses the given reversible circuit and checks for any possible application of rules R1-R7. This procedure is iterated until no further reduction is possible. This is because, the application of a rule may change a netlist in such a way that a subsequent application of rules is possible in a next iteration. For instance, if the initial netlist consists of positive control MCT gates only, then just rules R1, R5 or R7 can be applied during the first iteration. However, some negative control gates may get added to the netlist during the process, so that also the other rules may become applicable in the subsequent iterations.

Besides that, the order in which the respective gates of a template occur in a circuit does not matter as long as the lines with control connections are disjoint from the lines with target connections. Then, gates can be swapped without changing the function of the (sub-)circuit. This is because values on control lines are not modified by such a structure and the XOR operation on the target lines is commutative in general.

Overall, this leads to a procedure as sketched in Algorithm 1. The outer loop iterates through the gate netlist until no further rules can be applied. In each iteration, the function *find_seg* is invoked which identifies a segment G_{seg} in the gate netlist starting from *index* within which gates can be swapped (i.e. no control dots on the outputs). The function *apply_rule* checks the segment G_{seg} for applicability of the rules, considering the possible gate swappings, and applies a rule if a match is found. The iteration continues over the entire netlist. Finally,

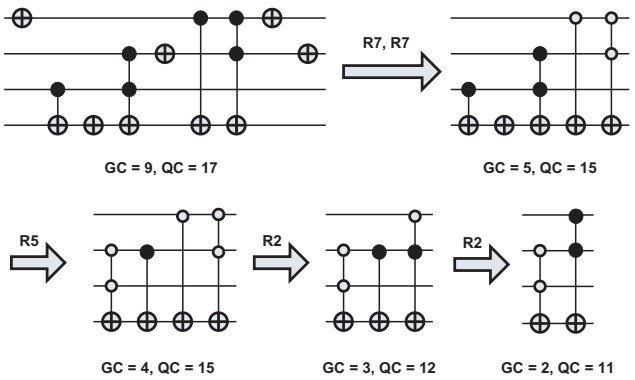


Fig. 2. Application of the proposed optimization

the netlist is compacted using the *compact_netlist* function. The time complexity of every iteration is linear in the number of gates.

The application of the algorithm is illustrated by the following example:

Example 2. Consider the reversible circuit depicted in the top-left corner of Fig. 2. In a first step, the NOT gates at the two top lines can obviously been removed. They only affect the positive control lines of the sixth and seventh gate which can simply be replaced by corresponding negative lines according to R7. Afterwards, the first three gates can be replaced by a smaller cascade according to R5, while R2 allows for the reduction of the last two gates. Finally, R2 allows for another reduction eventually leading to the circuit as shown in the bottom-right corner of Fig. 2. By this, the number of gates is reduced from 9 to 2 while the quantum costs are reduced from 17 to 11.

Due to the generic fashion of the rules, the approach described above can be applied to arbitrary circuits, i.e. realizations obtained by various synthesis approaches. However, our evaluations showed that the proposed methodology is particularly suited for circuits derived by ESOP-based synthesis [16–18]. Here, the targets lines are usually assumed to be placed on certain output lines, while control lines are usually placed on the separate input lines. By this, patterns as the ones from R1-R7 occur frequently.

5 Experimental Evaluation

This section provides experimental results for the proposed approach. To this end, the method and the rules described above have been implemented in C on top of *RevKit* [14] and applied to benchmarks circuits from the *RevLib* reversible logic website [22]. All experiments have been conducted on a Pentium dual-core desktop system with 4 GB of main memory running Ubuntu version 11.10.

Table 4 provides the results. The first columns denote thereby the name of the respective benchmark circuits (denoted by Circuit) together with its number of

Table 4. Experimental evaluation

Circuit	Lines	Original circuit		Optimized circuit		Impr. (%)	
		GC	QC	GC	QC	GC	QC
sf_274	5	19	155	7	143	63	8
rd32_273	5	20	116	8	104	60	10
rd53_131	7	28	119	12	104	57	13
sym10_262	11	194	25866	87	22717	55	12
9symml_195	10	129	14193	58	12747	55	10
max46_240	10	107	5444	51	4498	52	17
alu4_201	22	1063	55388	523	46388	51	16
tial_265	22	1041	56203	516	47125	50	16
sf_276	5	16	152	8	144	50	5
life_238	10	107	6766	57	5740	47	15
f51m_233	22	663	37400	358	33316	46	11
sf_275	5	11	51	6	42	45	18
example2_231	16	157	5654	87	4767	45	16
mux_246	22	35	1078	20	804	43	25
ham15_298	45	153	309	100	290	35	6
mlp4_245	16	131	3753	93	3531	29	6
cm150a_210	22	53	1096	38	822	28	25
in0_235	26	338	20031	245	18988	28	5
dc2_222	15	75	1886	55	1777	27	6
f2_232	8	19	255	14	238	26	7
rd73_252	10	80	1143	60	1066	25	7

All results have been determined in less than one CPU second.

lines (denoted by Lines). Afterwards, the gate count (denoted by GC) and the quantum costs (denoted by QC) of the original circuit as well as the optimized circuits are provided. Finally, the last columns show the percentage improvement with respect to the gate count and the quantum costs. *All* results have been determined in less than one CPU second. Because of this, a detailed listing of the run-time for the respective benchmarks is omitted.

The results clearly show the effect of the proposed rules to the size of the corresponding circuits. Improvements of almost up to two-third can be achieved. Even for large circuits composed of more than 1,000 gates a reduction of half the number of gates can be observed (see e.g. *alu4_201* or *tial_265*). Considering that these results have been generated in almost no run-time, this represents a worthwhile achievement. Similar template matching algorithms such as the one proposed in [9] usually require significantly more computation time and lead to a smaller reduction.

Moreover, also the resulting quantum costs of the circuits can considerably been reduced. Here, improvements of up to 25% (e.g. for *mux_246*) are reported – in many cases we see reductions of 10-20%. Note that alternative synthesis approaches such as the one proposed in [20] indeed reduced the number of gates using negative control lines, but were not able to reflect this improvement to the

quantum costs. In fact, quantum costs increased in the results shown in [20]. Using the approach proposed in this paper, we achieve substantial improvements with respect to both, number of gates and quantum costs. Besides that, determining better mappings of Toffoli circuits including negative control lines is subject to ongoing research (see e.g. [23, 24]). Thus, we expect better mappings and accordingly better quantum costs here.

6 Conclusions

In this work, we presented a post-synthesis optimization approach for reversible circuits which explicitly exploits the functional power of negative control lines. For this purpose, we analyzed that certain structured cascades of positively controlled Toffoli gates often subsume into a single negatively controlled Toffoli gate. Based on these observations, generalized rules have been derived which are applied in order to reduce the size of the given circuits. An experimental evaluation confirmed that the proposed approach leads to substantial reductions in both, the number of gates as well as the quantum costs. As a future work better gate reordering and template matching mechanism can be implemented to provide further reduction in gate count and quantum cost.

References

1. R. Landauer. Irreversibility and heat generation in computing process. *Journal of IBM Research and Development*, 5:183–191, 1961.
2. C. H. Bennett. Logical reversibility of computation. *Journal of IBM Research and Development*, 17:525–532, 1973.
3. R. Wille, R. Drechsler, C. Oswald, and A. Garcia-Ortiz. Automatic design of low-power encoders using reversible circuit synthesis. In *Design Automation Test in Europe*, pages 208–212, 2012.
4. M. Nielsen and I. Chuang. *Quantum Computation and Quantum Information*. Cambridge University Press, 2000.
5. D. Maslov, G. W. Dueck, and D. M. Miller. Techniques for the synthesis of reversible Tofolli networks. *ACM Trans. on Design Automation of Electronic Systems*, 12(4):42.1–42.28, 2007.
6. R. Wille and R. Drechsler. BDD-based synthesis of reversible logic for large functions. In *Design Automation Conference*, pages 270–275, 2009.
7. D. Grosse, R. Wille, G. W. Dueck, and R. Drechsler. Exact multiple control Toffoli network synthesis with SAT techniques. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 28(5):703–715, May 2009.
8. K. Datta, G. Rathi, I. Sengupta, and H. Rahaman. Synthesis of reversible circuits using heuristic search method. In *Intl. Conference on VLSI Design*, pages 328–333, 2012.
9. D. Maslov, G. W. Dueck, and D. M. Miller. Toffoli network synthesis with templates. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 24(6):807–817, 2005.
10. M. Soeken, R. Wille, G. W. Dueck, and R. Drechsler. Window optimization of reversible and quantum circuits. In *Symposium on Design and Diagnostics of Electronic Circuits and Systems*, pages 341–345, 2010.

11. T. Toffoli. Reversible computing. *Automata, Languages and Programming. Springer, Tech. Memo-MIT/LCS/TM-151, MIT Lab for Comp. Sci*, 1980.
12. E. Fredkin and T. Toffoli. Conservative logic. *Inernational Journal of Theoretical Physics*, 21:219–253, 1982.
13. A. Barenco, H. H. Bennett, R. Cleve, D. P. DiVinchenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter. Elementary gates for quantum computation. *Physical Review A (Atomic, Molecular, and Optical Physics)*, 52(5):3457–3467, 1995.
14. M. Soeken, S. Frehse, R. Wille, and R. Drechsler. RevKit: An open source toolkit for the design of reversible circuits. 7165:64–76, 2012. RevKit is available at www.revkit.org.
15. D. Michael Miller and Zahra Sasanian. Recent developments on mapping reversible circuits to quantum gate libraries. In *Int'l Symposium on Electronic System Design (ISED)*, dec 2012.
16. K. Fazel, M. A. Thornton, and J.E. Rice. ESOP-based Toffoli gate cascade generation. In *Pacific Rim Conference on Communications, Computers and Signal Processing*, pages 206–209, 2007.
17. Y. Sanaee and G. W. Dueck. ESOP-based Toffoli network generation with transformations. In *Intl. Symposium on Multiple-Valued Logic*, pages 276–281, 2010.
18. R. Drechsler, A. Finder, and R. Wille. Improving ESOP-based synthesis of reversible logic using evolutionary algorithms. In *Intl. Conference on Applications of Evolutionary Computation*, pages 151–161, 2011.
19. M. Soeken, R. Wille, C. Hilken, N. Przigoda, and R. Drechsler. Synthesis of reversible circuits with minimal lines for large functions. In *Asia and South Pacific Design Automation Conference*, pages 85–92, 2012.
20. R. Wille, M. Soeken, N. Przigoda, and R. Drechsler. Exact synthesis of Toffoli gate circuits with negative control lines. In *Intl. Symposium on Multi-valued Logic (ISMVL)*, pages 69–74, 2012.
21. K. Datta, I. Sengupta, and H. Rahaman. Group theory based reversible logic synthesis. In *International Conference on Computers and Devices for Communication (CODEC)*, December 2012.
22. R. Wille, D. Grosse, L. Teuber, G. W. Dueck, and R. Drechsler. Revlib: An online resource for reversible functions and reversible circuits. In *Intl Symp. on Multi-Valued Logic*, pages 220–225, 2008.
23. C. Moraga. Hybrid Reed Muller – de Morgan expressions for reversible computing circuits. In *Workshop on Reversible Computing (RC)*, pages 155–162, July 2011.
24. Z. Sasanian, R. Wille, and M. Miller. Realizing reversible circuits using a new class of quantum gates. In *Design Automation Conference 2012*, pages 36–41, 2012.