

Nearest-Neighbor and Fault-Tolerant Quantum Circuit Implementation

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Abstract—The quest of achieving higher computing performance is driving the research on quantum computing, which is reporting new milestones almost on a daily basis. For practical quantum circuit design, fault tolerance is an essential condition. This is achieved by mapping the target functions into the Clifford+T group of elementary quantum gates. Furthermore, the application of error-correcting codes in quantum circuits requires the quantum gates to be formed between adjacent Qubits. In this work, we improve the state-of-the-art quantum circuit design by addressing both of the above challenges. First, we propose a novel mapping of Multiple-Control Toffoli (MCT) gates to Clifford+T group gates, which achieves lower gate count compared to earlier work. Secondly, we show a generic way to convert any Clifford+T circuit into a nearest neighbor one. We validate the efficacy of our approach with detailed experimental studies.

Keywords— Quantum Cost, MCT (Multiple Control Toffoli), Clifford+T groups, NNC (Nearest Neighbor Cost)

I. INTRODUCTION

Quantum computing [1-2] is one of the most promising computing technologies with established theoretical results proving that there exists a significant gap between the classical and quantum computing [3]. In terms of practical realization, new capabilities in devices [4] and circuits [5] are being reported on a regular basis.

Quantum circuits are realized by several technologies such as, Ion Trap [6], Nuclear Magnetic Resonance (NMR) [7], Kane model [8] and superconducting circuits [9]. In a recent breakthrough, 2-qubit quantum gates have been realized in Silicon [10]. One of the major hindrances towards practical quantum circuit realization is fault-tolerance [11]. This is addressed at the logic level with fault detection strategies [12]. At the circuit level, error correcting codes are combined with physical qubits to provide maximum fidelity. Consequently, the universal operator set of Clifford+T [13] is chosen as the most suitable set due to the known constructions of Clifford group of operators and T gate for most promising error correcting codes, including surface codes. For surface codes, it is also necessary that the entangled gates are arranged in a nearest neighbor fashion. Therefore, an efficient mapping of a given function to a Clifford+T circuit with nearest neighbor construction is an important design challenge.

A. Preliminaries

Definition 1: The quantum state of a qubit $|\psi\rangle$ is the superposition of the two basic states $|0\rangle$ and $|1\rangle$ which is

defined as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α and β are the complex numbers that define probability values for states $|0\rangle$ and $|1\rangle$, respectively, such that $|\alpha|^2 + |\beta|^2 = 1$.

Each of the quantum gates, which are represented by unitary matrices, act on qubits. For a k -qubit quantum gate, the size of the unitary matrix is $2^k \times 2^k$. The number of qubits in the input and output of the gate are the same and all quantum gates are functionally reversible. The functionality of each quantum gate is obtained by multiplying the unitary transformation matrix with the quantum state vector.

In Table 1, we show some of the common single-qubit and two-qubit quantum gates together with their operational behavior.

Definition 2: A quantum gate library is a collection of quantum gates like NOT, CNOT, V/V^+ , W/W^+ etc. that performs the logical mapping between quantum gates to universal reversible gates (MCT gates).

NCV, NCVW, $NCV|v_1\rangle$ are well known gate libraries [14-17] that can realize MCT gates. For example, a quantum gate realization of the two control Toffoli gate using the NCV gate library is shown in Fig. 1(a).

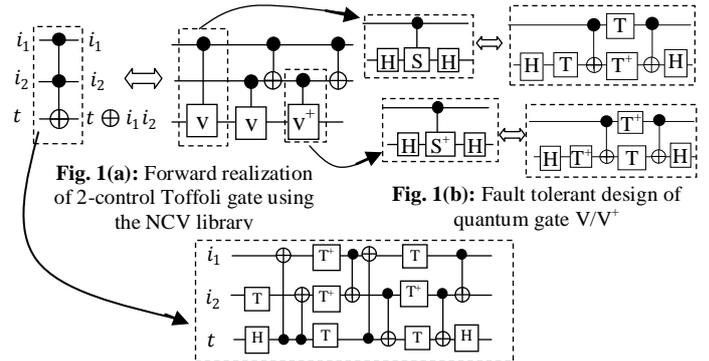


Fig. 1 (a): Forward realization of 2-control Toffoli gate using the NCV library

Fig. 1(b): Fault tolerant design of quantum gate V/V^+

Fig. 1 (c): Fault tolerant design of Fig.1(a) using Clifford + T group

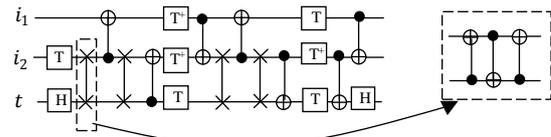


Fig. 1(d): Fault tolerant NNC free design of Fig.1(c) using naive approach

Definition 3: A fault tolerant circuit is a circuit that can continue un-interrupted performance when faults are developed in the circuit.

A fault-tolerant quantum circuit is such that, where Phase gates (S) in the circuit is free from control nodes. Using Clifford+T group, designing such a circuit is possible. In the Clifford group, gates such as Hadamard gate (H), Pauli's Z gate, Phase gate and CNOT gate are included. Besides that, also so-called T/T^+ gates are additionally included.

The fault tolerant design of a V/V^+ gate is shown in Fig. 1(b). By mapping each of the quantum gates present in an MCT structure, an equivalent fault tolerant design can be obtained. The equivalent fault tolerant design of Fig. 1(a) is depicted in Fig. 1(c). Some well-known metrics that are considered to measure performance of a fault tolerant design are stated below.

Definition 4: The quantum cost (QC) of a gate (g) is the number of elementary quantum operations performed to design the specified gate (g).

Definition 5: The T-count value of a circuit is the number of T/T^+ gate used to realize the input circuit.

Definition 6: The amount of time that is required to obtain the first output after applying an input to a T gate is termed as T-cycle.

Definition 7: The minimum number of T-cycles that are required to execute all T operations in a fault tolerant circuit is termed as T depth.

Definition 8: The number of gates in the circuit is called gate count.

Definition 9: Number of cycles used to execute the entire circuit is termed as circuit depth.

Definition 8: The Nearest Neighbor Cost (NNC) of a quantum circuit is defined as the sum of the NNCs of its gates; where for a quantum gate (g) having control at c^{th} line and target at t^{th} line has the NNC value $|c-t-1|$. An NNC free circuit always has either 1-qubit or 2-qubit gates in its configuration which operates on adjacent qubits by producing 0 Nearest Neighbor Cost.

The NNC free design of Fig. 1(a) using a naive approach is given in Fig. 1(d).

B. Related Work and Contribution

Though Clifford group [18, 19] of operators has the ability to produce fault-tolerant circuits, it is not a universal operator set and, therefore, a non-Clifford gate T is added to the existing Clifford group and a new fault tolerant group Clifford+T is formed.

Several design and automation approaches for constructing fault tolerant circuits using Clifford+T group are reported in [20-23], where the researchers have mainly studied the minimization of circuit size (T count, Gate count) and run time parameters (circuit depth, T depth).

In a recent work [21], the authors have shown a heuristic approach to design fault tolerant MCT structures using the Clifford+T group. But the authors have restricted their work up-to 3-control MCT gates due to the increasing complexity of the approach.

Moreover, for the physical realization of these fault-tolerant quantum circuits, NNC free designs of such circuits are another important requirement which is not studied in [21]. The most common way of converting a quantum circuit to a NNC free one, is by inserting SWAP gates. However, in order to minimize the overall cost of the circuit, appropriate SWAP sequences have to be incorporated and to achieve further minimization in the NNC free design, post synthesis schemes [24-28] have been proven very efficient. In [29], a template matching technique is proposed, which replaces the SWAP insertion scheme and reports suitable results with respect to NNC reduction. Although the presented scheme works for Clifford+T circuits, it has not been applied to the MCT mappings proposed in [21].

In this work, we show that an improved mapping of MCT gates to NNC free Clifford+T circuit is possible.

TABLE 1: QUANTUM GATES AND THEIR PROPERTIES

Type (symbol)	Matrix	Diagram	Properties	Type (symbol)	Matrix	Diagram	Properties
NOT (X)	$\begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$		$X 0\rangle = 1\rangle$ $X 1\rangle = 0\rangle$	Pauli-Y	$\begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}$		$Y.Y = I$ $Y 0\rangle = 0\rangle$ $Y 1\rangle = -i 0\rangle$
CNOT (C)	$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$		$t_{out} = t \oplus c$	Pauli's Z	$\begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$		$Z.Z = I$ $Z 0\rangle = 0\rangle$ $Z 1\rangle = - 1\rangle$
Controlled V ($V = \sqrt{N}$)	$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} \\ 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} \end{pmatrix}$		$V^* = V^{-1}$	Controlled V^+ ($V^* = \sqrt{N}$)	$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} \\ 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} \end{pmatrix}$		$V.V^* = I$
Hadamard (H)	$\frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$		$H 0\rangle = \frac{1}{\sqrt{2}}(0\rangle + 1\rangle)$ $H 1\rangle = \frac{1}{\sqrt{2}}(0\rangle - 1\rangle)$	S^+ gate	$\begin{pmatrix} 0 & 1 \\ 1 & e^{-i\pi/2} \end{pmatrix}$		$S 0\rangle = 0\rangle$ $S^+ 1\rangle = e^{-i\pi/2} 1\rangle$
T gate	$\begin{pmatrix} 0 & 1 \\ 1 & e^{i\pi/4} \end{pmatrix}$		$T 0\rangle = 0\rangle$ $T 1\rangle = e^{i\pi/4} 1\rangle$	Phase S gate (\sqrt{Z})	$\begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/2} \end{pmatrix}$		$S = \sqrt{Z} = H.V.H$ $V = H.Z.H$
T^+ gate	$\begin{pmatrix} 0 & 1 \\ 1 & e^{-i\pi/4} \end{pmatrix}$		$T^+ 0\rangle = 0\rangle$ $T^+ 1\rangle = e^{-i\pi/4} 1\rangle$	Phase T gate	$\begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/2} \end{pmatrix}$		$T = H.\sqrt{V}.H = H.W.H$ $W = H.T.H$
S gate	$\begin{pmatrix} 0 & 1 \\ 1 & e^{i\pi/2} \end{pmatrix}$		$S 0\rangle = 0\rangle$ $S 1\rangle = e^{i\pi/2} 1\rangle$	Phase T+ gate	$\begin{pmatrix} 1 & 0 \\ 0 & e^{-i\pi/2} \end{pmatrix}$		$T^+ = H.\sqrt{V^*}.H = H.W^*.H$ $W^* = H.T^*.H$
Controlled S gate	$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & i \end{pmatrix}$			Controlled S^+ gate	$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -i \end{pmatrix}$		

This is achieved by a set of templates for higher order MCT gates (we demonstrate this for up to 5-control lines) and NNC reduction by considering the *linear nearest neighbor* (LNN) property for CNOT gates. Our combined approach improves the circuit performance significantly.

The rest of the paper is organized as follows. The proposed technique with examples is discussed in Section II. Section III deals with the experimental results and final concluding remarks appear in Section IV.

II. PROPOSED TECHNIQUE

Here we discuss the improved design methodology for constructing NNC free and fault tolerant MCT structures. The entire design procedure is composed of two phases.

In the first phase, we have modified the algorithm of [21] and have incorporated a circuit optimization procedure aiming for better mapping of MCT gates to Clifford+T structures. First, we execute a *heuristic template matching* scheme over the quantum circuits, followed by two steps of *phase gate reordering* and *redundant gates cancellation* which together improve our design in comparison to the existing approach [21]. In the next phase, we have restructured the designs to make them NNC free.

Phase 1: Improve mapping scheme for fault tolerant designs of NCV based MCT gates:

Before stating the entire scheme, here we are defining a template which is extensively in our proposed mapping procedure.

Template 1: The defined template (as shown in Fig. 2(a)) is composed of a pair of Toffoli gates in which both the gates have the same control lines (c_0 and c_1) that act on the same target line (t). Mapping of each of the Toffoli gate to its fault tolerant structure does not lead to an optimization, and for that we have chosen a strategy to map both the Toffoli gates jointly into a fault tolerant one. We have appended the redundant CNOT gates to the initial structure in Fig. 2(b) and then find its optimized NCV-based quantum circuit after eliminating the redundant gates as depicted in Fig. 2(c). Then we map each V/V^+ gates to its equivalent Clifford+T group based sub-circuits. Next, we apply the possible transformation rules that have been defined in Table 2 over the circuit followed by cancellation of redundant gates present in the circuit.

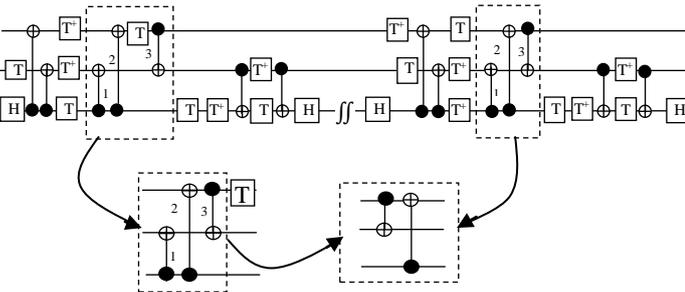
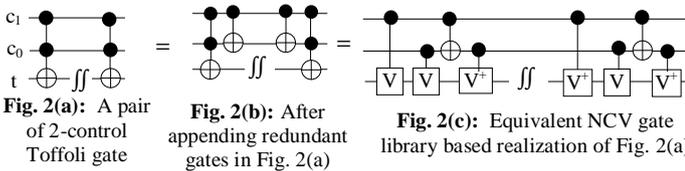


Fig. 2(d): Reordering and then removing extraneous gates from the circuit

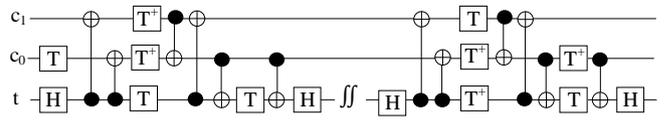


Fig. 2(e): Clifford+T based fault tolerant realization of Fig. 2(a) after optimization

The intermediate design is presented in Fig. 2(d). The final fault tolerant structure corresponding to Fig. 2(a) is obtained and has been shown in Fig. 2(e).

Now we present the proposed mapping scheme, which is composed of seven steps:

Step1: Take an MCT gate (G) out of which a fault-tolerant design is to be obtained.

Step2: Realize this gate as an NCV quantum gate circuit using the approach introduced in [14].

Step3: The obtained circuit contains elementary quantum gates like NOT, CNOT, V/V^+ and Toffoli gates. Now, scan the circuit from left to right and replace all the V/V^+ gates with its equivalent Clifford group based sub-circuits.

Step4: Reorder the circuit as per the rules stated in Table 2.

Step5: Next, substitute all the controlled-Phase gates (S) existing in the circuit with equivalent control free Phase gates. Now, the circuit is composed of Hadamard gates (H), Clifford T/T^+ , CNOTs gates and a pair of two-control Toffoli gates.

Step6: As the present circuit contains a pair of 2-control Toffoli gate, it is necessary to replace that structure with an equivalent Clifford+T-based fault tolerant sub structure (Template1). To this end, substitute the sub-circuit as in Fig. 2(a) present in the circuit with the equivalent fault tolerant sub structure of Fig. 2(e).

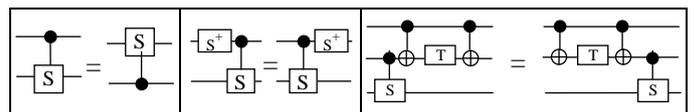
Step7: Apply the following two circuit optimization rules in the circuit:

Step7.1: As the product of two H-gates is the identity remove two consecutive H-gates from the structure.

Step7.2: Move phase gates (T/T^+) across the control node of CNOT gates such that T-depth minimizes but no movements of phase gates are allowed across the target line of NOT or CNOT gates. Otherwise, the functionality of the entire circuit will get modified.

Step7.3: Interchange the control line and target line of two qubit phase gates when it is necessary according to rules defined in Table 2.

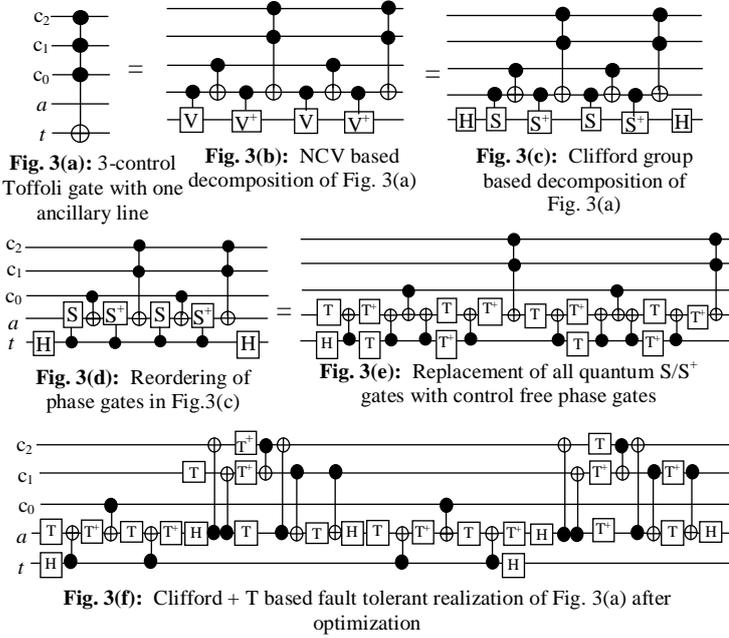
TABLE 2: SOME IMPORTANT TRANSFORMATIONS



For better understanding of the entire design procedure, consider the following example, where the improved fault tolerant design of a 3-control Toffoli gate is discussed.

Example 1: Initially, the 3-control Toffoli gate which is depicted in Fig. 3(a) is decomposed using the mapping technique stated in [14]; leading to the circuit in Fig. 3(b). Now, by replacing all the V/V^+ gates to its equivalent Clifford group based sub-circuits, the resulting structure shown in Fig. 3(c) is derived. Next, we reorder the phase gates in Fig. 3(c)

and obtain the modified design in Fig. 3(d). Then, replacing all the Phase gates (S) in Fig. 3(d) with equivalent Clifford +T based fault tolerant sub-circuits yields the circuit given in Fig. 3(e). While reviewing the circuit of Fig. 3(e), we found a sub-structure that matches the template in Fig. 2. So, substitute the sub-structure with Template1 and all the redundancies are removed from the design as per the principle stated in Step7. Finally, in Fig. 3(f), the obtained and improved fault tolerant design of the three control Toffoli gate is shown.



Phase 2: Making Clifford+T structures NNC free:

Above, we have shown how to make a quantum circuit fault tolerant using Clifford+T group gates and have also formulated the strategies to improve the cost metrics of that circuit. In this phase, we process the circuits that have been obtained after executing *step5* from the previous section in order to make them NNC free.

As stated in Section I, there already exist several well-known techniques to make any arbitrary circuit NNC free. Most of the approaches apply template matching schemes followed by a local and a global reordering scheme of gates to make the circuit NNC free. But as these approaches need some serious computation, the complexity of this approach quickly increases.

Here we are showing an easier way to make our fault tolerant circuits NNC free using two simple templates that replace the non-NNC free gates or sub-circuits with equivalent NNC-free sub-structures. Interestingly, it can be noted that using any of the well-known NNC optimization techniques for the fault-tolerant circuits considered here would yield the same result. However, in order to reduce the complexity, we have used the defined templates and associated strategy as proposed in this work.

As the present circuit contains H gates, T/T⁺ gates, CNOT gates and pair of two control Toffoli gates in its design, where all the H gates and T/T⁺ gates in the circuit maintain physical adjacency between the two neighboring lines. That means they all are NNC free structures. But the CNOT gates and the pair of Toffoli gates that are present in the design are not NNC free

structures and we have to make them NNC free to retain the entire design's NNC at zero.

To this end, we are utilizing the following templates:

Template2: A CNOT gate having one ancillary line has to be replaced with the template as defined in Fig. 4.

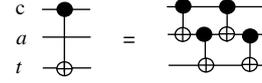


Fig. 4: A CNOT gate and its NNC free design

Template3: The NNC free fault-tolerant design of a pair of ancilla free 2-control Toffoli gates is given in Fig. 5. Initial diagram of the Toffoli gate is depicted in Fig. 5(a). After going through three intermediate stages (Fig. 5(b) to Fig. 5(d)), the final design is obtained in Fig. 5(e).

But if the pair of 2-control Toffoli gates contains ancillary lines, n for example, then the structure will be a bit different. For this scenario, first we have to decompose the initial structure using the previously defined *template2* so that the decomposed design becomes NNC free. Though externally this decomposed design looks NNC free, it is not as it contains a pair of ancilla free 2-control Toffoli gates which are not NNC free. So, we have to substitute this pair of 2-control Toffoli gates with the NNC free fault-tolerant structure that we have defined earlier (in Fig. 5).

The above stated idea is explained in Fig. 6, where the initial design of a pair of 2-control Toffoli gates containing n ancillary lines and its decomposed structure are depicted in Fig. 6(a) and Fig. 6(b), respectively. After substituting the pair of ancilla free 2-control Toffoli gates (shown in the dotted box) in Fig. 6(b) with NNC free fault tolerant structure of Fig. 5, the final NNC free fault tolerant design of Fig. 6(a) is obtained in Fig. 6(c).

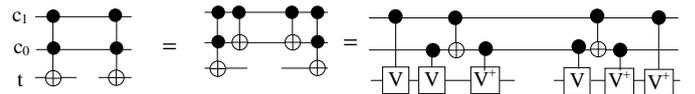


Fig. 5(a): A pair of 2-control Toffoli gate

Fig. 5(b): Appending two CNOT gate in Fig. 5(a)

Fig. 5(c): Equivalent NCV realization of Fig. 5(b)

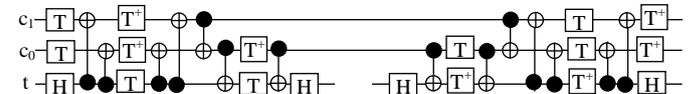


Fig. 5(d): Replacing all quantum V/V^+ gate by its equivalent Fault tolerant structure

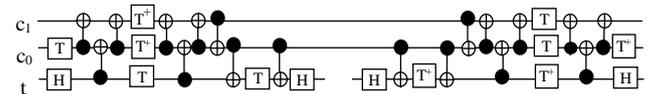


Fig. 5(e): NNC free structure of Fig. 5(a)

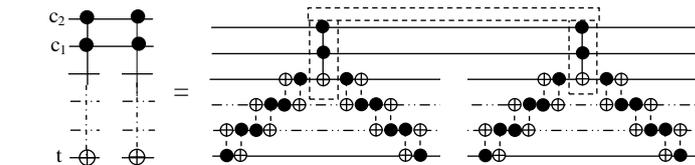


Fig. 6(a): Pair of 2-control Toffoli gates with n ancillary lines

Fig. 6(b): NNC free decomposition of Fig. 6(a)

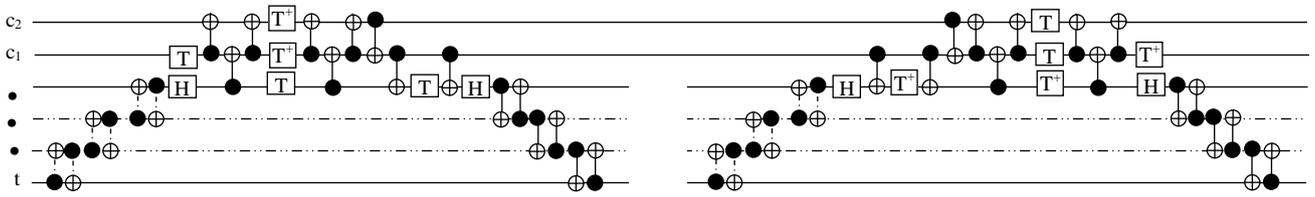


Fig. 6(c): Optimized NNC free structure of Fig. 6 (a)

If the defined templates are mapped over the fault tolerant design of three controls Toffoli gate in Fig. 3(e), then the circuit will be transformed into a NNC free design and after applying optimization rules over it finally Fig. 7 is obtained.

Example 2: The NNC free fault tolerant structure of a 5-control MCT gate is shown in Fig. 8. The initial design of the MCT gate is depicted in Fig. 8(a). Fig. 8(b) presents the fault tolerant realization of the gate. After removing all the non NNC based gates from the circuit, the final fault-tolerant NNC free design is given in Fig. 8(c).

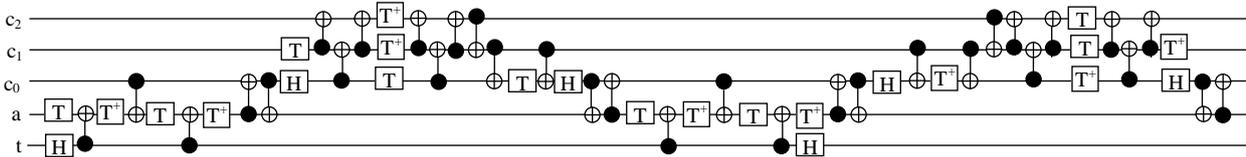


Fig. 7: NNC free fault tolerant design of 3-control MCT gate

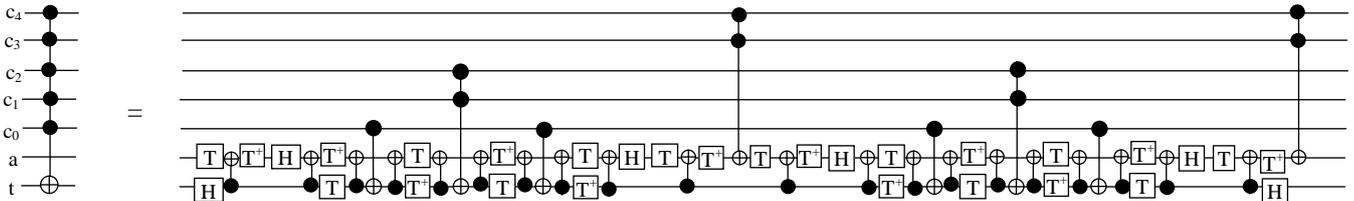


Fig. 8(a): 5-control MCT gate

Fig. 8(b): Equivalent fault tolerant design of Fig. 8(a)

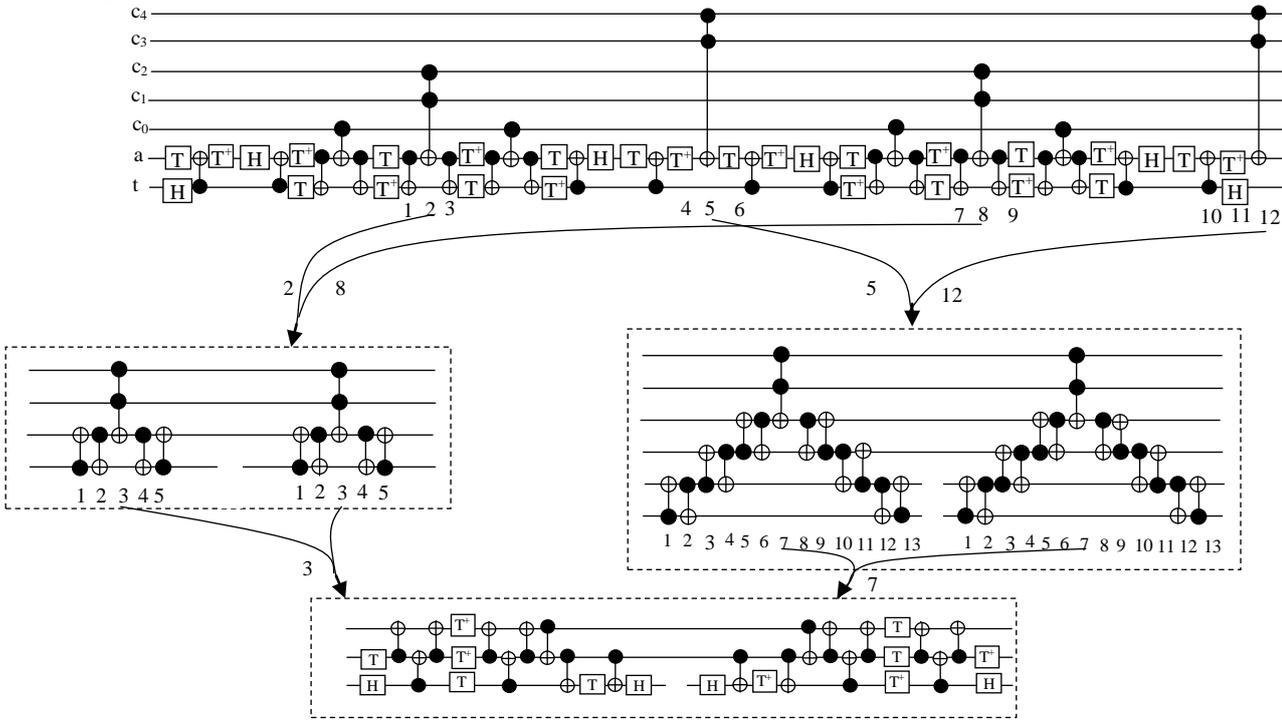


Fig. 8(c): NNC free fault tolerant design of 5-control MCT gate

III. EXPERIMENTAL RESULTS

Here we give two sets of results in two separate tables – Table 3 and Table 4 where we have shown various cost metrics after applying our entire approach over MCT gates and benchmark circuits [30]. We have compared our results with [21] where fault tolerant circuits are designed followed by NNC free technique as stated in [29]. Percentage improvements in both the tables are calculated and are shown. In Table 3, it can be observed that improvements are attained when MCT sizes increases but in that table for the first two rows improvements are not seen as the gates in the respective two rows do not have any ancillary lines.

TABLE 3: FAULT-TOLERANT NNC FREE DESIGN OF MCT GATES

No. of control lines	Cost metrics obtained using technique [21] followed by [29]				Proposed design cost metrics				% Improvements	
	QC	TC	GC	CD	QC	TC	GC	CD	QC%	CD%
0	1	0	1	1	1	0	1	1	0	0
1	1	0	1	1	1	0	1	1	0	0
2	20	7	20	13	19	7	19	13	5	0
3	62	18	62	49	56	18	56	46	9	6
4	102	28	102	81	94	28	94	76	7	6
5	178	44	178	150	140	44	140	128	21	14.66
Average improvement									7	4

TABLE 4: COMPARATIVE ANALYSIS USING BENCHMARK CIRCUITS

Benchmark names	Cost metrics obtained using technique [15] followed by [21]				Proposed design cost metrics				% Improvements	
	QC	TC	GC	CD	QC	TC	GC	CD	QC	CD
n	QC	TC	GC	CD	QC	TC	GC	CD	QC	CD
mod5adder	438	99	438	319	417	99	417	313	4	1
permanent 2x2	160	42	160	121	150	42	150	116	6	4
main\2of5\design#1	514	125	514	416	475	125	475	396	7	4
bnhmrk_1	281	72	281	232	235	72	235	205	14	11
bnhmrk_2	342	90	342	280	290	90	290	250	15	10
bnhmrk_3	198	51	198	163	159	51	159	141	19	13
Average improvement									11	7

QC: Quantum Cost TC: T-Count GC: Gate Count
 CD: Circuit Depth n: No. of control lines

IV. CONCLUSION

In this work, we have proposed an improved design technique for constructing NNC free fault tolerant quantum circuits relying on the Clifford +T library for MCT gates. The proposed scheme has two phases. In the initial phase, we have improved the mapping scheme from MCT gates to its fault-tolerant design by reducing gate count and circuit depth, while in the second phase, we have made these circuits NNC free. In future work, we will investigate how to realize higher order MCT gates as NNC free fault tolerant quantum circuits.

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