Machine Learning Based Test Pattern Analysis for Localizing Critical Power Activity Areas

Harshad Dhotre* Stephan Eggersglüß*† Mehdi Dehbashi‡ Ulrike Pfannkuchen‡ Rolf Drechsler*†
*Institute of Computer Science, University of Bremen, 28359 Bremen, Germany
†Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany
‡Infineon Technologies AG, Munich, Germany
dhotre@uni-bremen.de, segg@informatik.uni-bremen.de, drechsler@uni-bremen.de

***Abstract*—The identification of power-risky test patterns is a crucial task in the design phase of digital circuits. Excessive test power could lead to test failures due to IR-drop, noise, etc. This has to be avoided to prevent yield loss and chip damages. However, the accurate power simulation of all test patterns to identify power-risky patterns as well as to find critical areas within each pattern is not possible due to run time and resource constraints. An important task is therefore the selection of a subset of potentially power-risky patterns, which will be simulated in an accurate manner. In this paper, we propose an independent test pattern analysis methodology for the integration into an existing industrial design flow. The proposed test pattern analysis technique is a lightweight method based on the cell's Transient Power Activity (TPA) to identify potentially power-risky patterns. The method uses layout and power information to identify critical power activity areas using machine learning techniques. Experiments were performed on opensource benchmarks as well as on an industrial design. The results were correlated with commercial power and IR-drop simulation tools. The proposed methodology was found to be effective in terms of speed and localization of the critical areas for unsafe patterns.**

I. Introduction

Power safe testing has become very important in the development and manufacturing of state-of-the-art circuits. The high density and reduced feature sizes in integrated circuits make testing of manufactured IC's more difficult. Tools for *Automatic Test Pattern Generation* (ATPG) generate high quality test patterns in terms of test coverage, test data volume and testing time. However, the generated test patterns can have a larger amount of transitions as compared to the functional mode. This may result in damaged devices or false testing results, which, in turn, reduces the yield. Typically, ATPG tools use the *Weighted Switching Activity* (WSA) metric to approximate the power consumption of test patterns. Basically, the WSA metric sums up all toggles on signals and branches. The ATPG tool usually does not consider any technological information during test generation due to the increase in complexity and the ATPG run time. Some of the high quality test generation methods consider the WSA as criteria for low power pattern generation, peak power drop and IR-drop estimation [15], [18]. Other test generation techniques also consider probabilistic information and constraint based approaches for low power test generation [2], [17]. The WSA is mostly indicated in term of numbers, rating the patterns and some commercial tools provide this information in terms of percentage of the maximum WSA value.

The WSA metric is highly approximate and is insufficient for power estimation and IR-drop analysis. The analysis has to be done separately in the design flow and is a very important signoff stage in the industrial tool flow to find unsafe and power-risky patterns. However, there are the following problems, which are addressed in this paper:

- An accurate test power analysis is highly time-consuming. The power as well as IR-drop analysis tools perform rigorous calculations with the help of cell and technology libraries. In practice, this accurate simulation is only possible for a few test patterns due to run time constraints in the later development stage.
- The pre-selection for test patterns, which are to be accurately power-simulated is mainly based on approximate metrics such as WSA or even done randomly. However, the existing approximation metrics are not dependable enough. Therefore, there is a need for a more effective and dependable as well as a fast metric for pattern pre-selection.
- Besides the general global switching activity, the identification and incorporation of localized peak power estimation becomes more and more important within the pattern. The power critical areas or concentrated switching activity areas on the layout need to be identified dynamically on the layout.

In this paper, we propose a lightweight method to grade the generated test patterns based on the cell library power information for the rise and fall transitions separately. These factors play an important role during the calculation of the proposed *Transient Power Activity* (TPA) value for each gate as well as for each pattern. The different number of rise transitions and fall transitions, thereby affects the calculation of the TPA value. Other approximation metrics such as WSA consider typically only the toggling information on the gate's output and (sometimes) weights it with the load capacitance or power-rail information [17]. The WSA calculation neglects the input transitions of the gate and the gate's internal switching.

The proposed method uses also the toggling number (as WSA) but is also input-dependent and, by this, reflects more the internal switching of the gate by using technology information. This method can therefore be used to pre-select potentially unsafe patterns for accurate simulation. Another important aspect to consider is the locality of the power consumption. The proposed approach uses layout information to correlate the determined TPA values to the actual circuit layout. Machine learning techniques, i.e. unsupervised clustering techniques, are used to dynamically determine regions of high-power consumption for each pattern. This enables a more reliable pattern pre-selection.

Section II discusses related work done in this field. Section III presents the proposed TPA metric, while Section IV shows the dynamic clustering results. The experimental results are given in Section V and conclusions are drawn in Section VI.

978-1-5386-0362-8/17/$31.00

II. Related Work and Background

Previous approaches for power estimation of test patterns were mainly based on fanout-based switching activity and probabilistic measures, which is highly approximate. The dominant approximation metric is WSA. The WSA of a test pattern can be calculated in the following way. Each signal in the circuit is associated to a WSA value. The WSA value of a node is the number of signal changes multiplied by $(c + N)$, where N is the number of fanouts and c is either 1 or represents the load capacitance of the signal. The WSA value of the circuit is the sum of all WSA of all nodes for one test. The higher the WSA value of a test, the more switching is supposed to occur. However, the WSA value is highly approximate since cell technology information is not incorporated.

The technique proposed in [13] identifies areas where IR-drop likely occurs, but it is based on the probability of switching activity at gate level and does not take the test patterns into account. The approaches [1], [5], [7]–[10] partition the circuit pattern-independently in static regions. This uniform partitioning is disadvantageous because it may not detect the high power activity areas at borders between the partitions, e.g. when a high power-consuming region is spread over more than one static partition. Hence, there is a need to introduce a dynamic partitioning approach, which clusters the high power activity areas depending on neighboring instances.

Another approach [19] identifies the peak current to determine the power-safe patterns. But this approach also partitions the layout in equal sizes and uses WSA to relate it to current limits and the WSA threshold. A similar approach was proposed in [11] to identify the power unsafe patterns and, afterwards, regenerate safe patterns. However, this method is based on the WSA metric. A further method for pattern grading based on WSA for critical paths is used in [12].

In industrial practice, the VCD based power and IR-drop simulation is performed for various scenarios for functional as well as test mode. But such kind of simulations are not feasible for all test patterns because of the required run time in a late design phase. Hence, a pre-selection of the worst and potentially risky test patterns is required.

III. Transient Power Acticity

This section introduces the TPA metric to assess the power dissipation of a test pattern. During IC development, cell libraries and technological data are used for the analysis of the design. These data contain information about timing, power, functionality, area, drive strength etc. The information is extensibly used for the design automation and analysis process by various EDA tools, but typically not for WSA calculation. The goal is to correlate this information to a switching activity based metric which takes the cell's internal switching into account. This makes it more accurate, but it still can be calculated very fast.

The cell power analysis boils down to the basic concept of power dissipation in digital circuits [14]. The total power is a combination of static power and dynamic power. The static power is small and mostly technology-dependent, while the dynamic power is dependent on the transitions in the cell and may vary according to the technology used and shown in Equation 1:

$$P_{Dyn} = \sum_{Cells} (P_{int \times Ei}) + \sum_{nets} (C_{load \times Ei} \times \frac{Vdd^2}{2}) \quad (1)$$

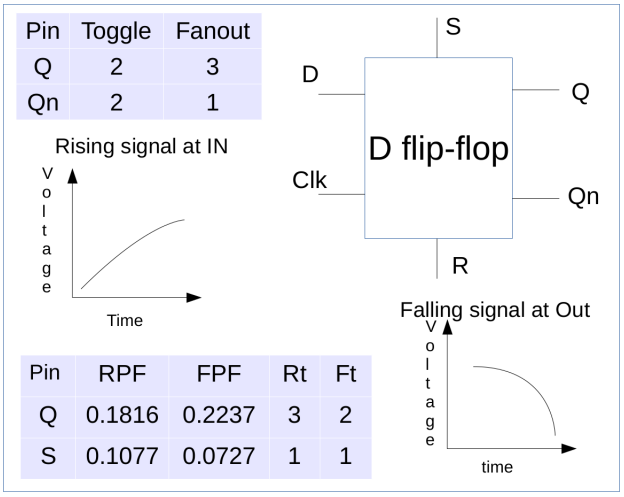

Fig. 1: Library cell

TABLE I: Comparison of Switching Power, TPA and WSA

Design unit	Instances	Toggles	WSA	Power	TPA
NAND2X1	8	4	32	2.749E-08	38.2694
NAND8X4	2	4	32	0.986E-08	12.3197

The TPA value involves the power factor calculation for the rise and fall transitions for each pin of each cell from the technology library to account for the cell internal switching. For each cell c and each pin p_c, the *Rise transition Power Factor* (RPF_{p_c}) as well as the *Fall transition Power Factor* (FPF_{p_c}) are extracted.

Each and every design unit instantiated in the design has its reference to the base cell and technology library for which these factors are calculated. These calculated power factors are used along with the number of rise and fall transitions occurring at each pin of each cell in the design to calculate the TPA value of the instantiated design unit. Therefore, logic simulation has to be carried out for each test t to record the number of rising transitions (Rt_{p_c}) as well as falling transitions (Ft_{p_c}) on each pin p_c which can be done using ATPG tools or with an accurate simulator considering timing information to account for glitches. The TPA value TPA_t for a test t is calculated for each shift cycle as well as for the capture cycle.

$$\text{TPA}_t = \sum_{Instance} \sum_{Pin} (\text{RPF}_{p_c} \times Rt_{p_c}) + (\text{FPF}_{p_c} \times Ft_{p_c}) \quad (2)$$

This calculation gives more accurate information related to transient power activity in each cell for each test pattern as compared to WSA, which is based on the fanout number and toggles at the gate's output. Example values for a D flipflop cell are illustrated in Figure 1. The standard D flipflop is shown in the figure along with the rise and fall time variations in voltage, which results in different power consumption during rise and falling edges. The (rise and fall) power factors are calculated based upon these different behaviors. In contrast to this, WSA does not distinguish between rise and fall toggles which makes it more inaccurate. Furthermore, the power factors have a quadratic function similar to the power consumption, while the WSA calculation uses a linear function based on the fanout.

As a further example, a comparison between WSA and TPA calculation is made for two gates cells, i.e. NAND2X1 and NAND8X4, which have a driving strength of 1 and 4, respectively. Assume that the first cell occurs 8 times and the second cell occurs 2 times, respectively. Further assume that

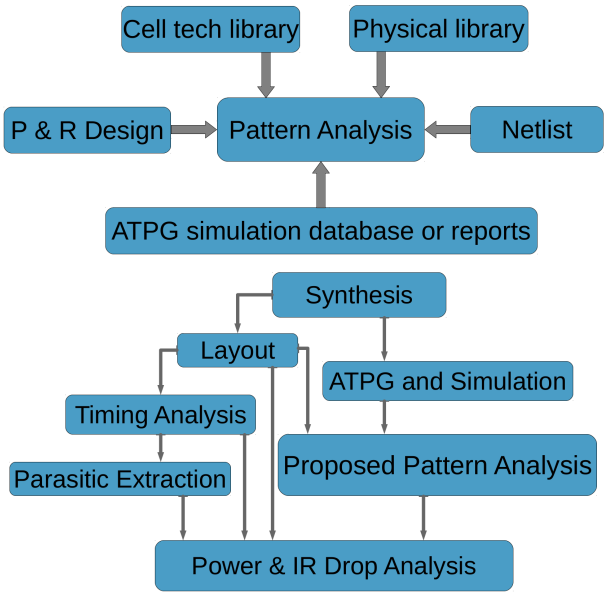

Fig. 2: Proposed methodology and flow

one test pattern produces 2 rise as well as 2 fall transitions on the outputs, i.e. 4 toggles. As a result, the WSA of both is 32 and exactly the same. But the switching power consumed by them is different since the technology data is different. This is accounted for using TPA. As a result, the TPA metric is more accurate than WSA.

Figure 2 shows the major blocks of the proposed TPA analysis and the incorporation into an existing design flow. The upper part shows the input of the proposed analysis, e.g. the design files, reports and libraries. All information is processed together to estimate the worst pattern and power critical areas. The lower part shows the integration of the proposed analysis in the design flow. It can be applied after the ATPG step, when the test patterns have been generated. For localizing critical areas, layout information has to be available. In summary, the following procedure is used to calculate the TPA values of a test set for pattern selection.

1) Extract the power factors for each cell and pin from the process technology data. Store them in a look-up table.
2) Simulate the generated test set with a circuit simulator (shift cycles and capture cycle). Record the number of rise and fall transitions for each instance and pin for each pattern. This can be further extended by using SDF timing information.
3) Calculate the TPA value for each pin of each instance using the RPF and FPF of the corresponding cell.
4) Sum up the TPA values for each pattern and cycle and rank the pattern based on these results.

The difference between TPA and WSA ranking is further illustrated by an example circuit. Consider the example design s27 shown in Figure 3, which includes one scan chain with 3 scan flipflops and 16 other gates. In total, 9 patterns were generated for 150 stuck-at faults. These patterns were analyzed and rated using the TPA metric as well as the WSA metric. The difference in the TPA and WSA ranked patterns can be seen in Table II. For instance *pattern3* is ranked highest in the TPA ranking, but ranked very low in the WSA ranking. This is especially important since the ranking is crucial for the pre-selection for an accurate power analysis. The validation of the TPA ranking will be given in Section V.

TABLE II: Pattern ranking for s27 design

Pattern	TPA	WSA	TPA_rank	WSA_rank
pattern0	7.786393	14	8	9
pattern1	7.993566	29	7	5
pattern2	10.707233	35	2	4
pattern3	10.891229	25	1	6
pattern4	10.577063	36	3	2
pattern5	8.702493	23	6	7
pattern6	6.767385	15	9	8
pattern7	9.273815	36	5	3
pattern8	9.445467	40	4	1

IV. Machine Learning Based Clustering

A ranking of the test patterns for pre-selection based on the global activity is not always sufficient. Local hot spots have to be considered, too. Although a test pattern could have a low or medium global TPA value, there can be regions with high concentrated power dissipation. Previous approaches account for this issue by partitioning the circuit layout in static regions. For each region, the power can be estimated separately, e.g. using the WSA metric. This cause problems since the regions have to be determined a priori and are pattern-independent. The different clustering techniques have been compared in [6].

In this paper, we propose to dynamically divide the layout depending on the power activity of each pattern using clustering. Layout information is used to assign the cell area and the corresponding x and y coordinates to each cell instance. The goal is to cluster all m instances $x_i = (x_1, ...x_m)$ in the design into k partitions/clusters (k is a parameter given by the user) such that the function for the centroids or means $m_1, m_2, \ldots, m_k$ is kept minimum or within cluster sum of square for dimensions d_k.

$$\sum_{k=1}^{K} \sum_{i \in d_k} ||x_i - m_k||^2 \tag{3}$$

The centroid is defined as the mean TPA density value of the clustered instances. The TPA density is defined as the TPA value divided by the area.

For clustering of the instances depending on their corresponding TPA, we used machine learning based unsupervised clustering technique, i.e. the k-means clustering algorithm [6], which is also often applied in image processing [3], [4], [16]. The input data of the algorithm is

- the design netlist and library files for power factors and the calculated TPA values for the instances
- the X and Y coordinates from the def file of each instance along with other necessary data from the corresponding lef file of the design unit
- other algorithm-specific settings like fixed cluster number, optimal cluster number, distance etc.

The k-means clustering algorithm partitions the layout into different clusters by aggregating the instances having similar TPA density values and are close to each other. The euclidean distance parameter is considered here for keeping the function minimum. The TPA density is calculated based on the TPA value of the instances and their corresponding area. The outcome of the algorithm is that instances, which have a similar TPA density and are close to each other are clustered in one partition. An arbitrary clustering is not possible because the maximum number of clusters is limited. The algorithm therefore optimizes the clusters according to the given objective.

The algorithm assigns the mean value of the TPA density to each cluster during the computation and gives the values as a result along with the mean X and Y coordinates of all instances in the cluster. These values are considered as centroid

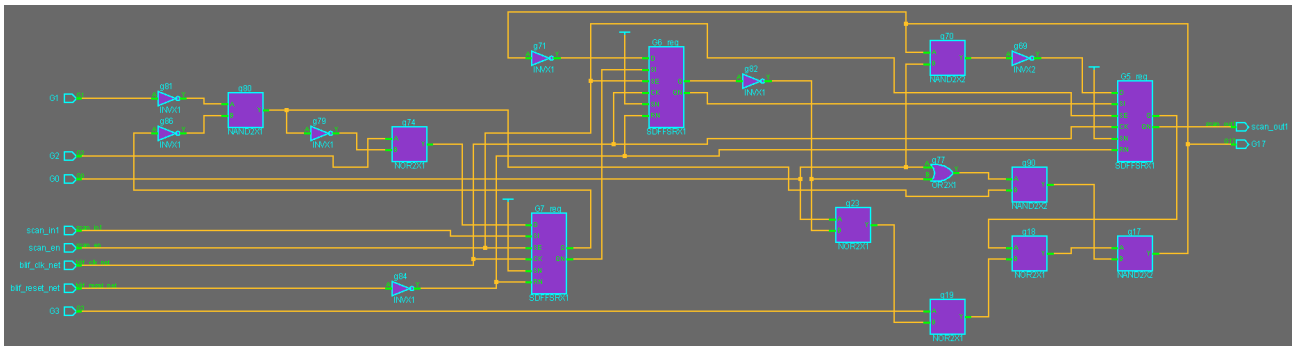

Fig. 3: Schematic of s27 design

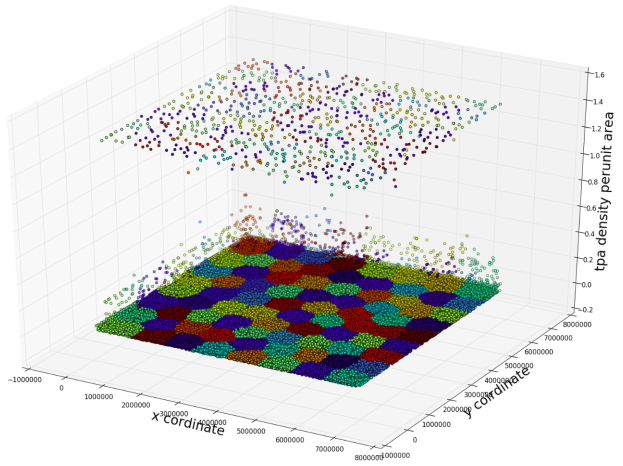

Fig. 4: TPA based clusters of Ethernet design

parameters and characterizes each cluster. This technique overcomes the drawback caused by static partitioning of the layout in equal blocks. Another advantage is that the border between clusters are formed such that instances of similar TPA values belong to the same partition, which is not the case when manual partitioning is applied. Figure 4 shows an example clustering for the application of one test pattern of the OpenCore Ethernet design. Since the TPA density of each cluster is assigned, critical areas can easily be identified.

V. Experimental Results

The experiments were performed on benchmarks circuits, i.e. OpenCores. We also verified the results on an industrial design using commercial tools within the design flow. The test patterns are generated and simulated using commercial tools. The power and IR-drop simulation were also performed in the industrial environment for the physical netlist using 40nm technology. For the OpenCores designs, a 180nm open source library was used. The clustering was done using Python.

TABLE III: Results for open source Ethernet design

Pattern	TPA	WSA
pattern14	16865210.3625013	5907618
pattern8	16768852.6945524	6162904
pattern20	16682560.0135287	5704496
pattern38	16588545.5000258	5548111
pattern19	16518086.7604578	5006614
pattern11	16482947.6841785	4661280
pattern30	16467017.7488741	5030147
pattern36	16459723.6733557	4954547
pattern34	16421653.9829964	4787670
pattern44	16354071.8754795	4401100

Table III shows experimental results for the OpenCore design Ethernet which has 10544 scan cells arranged in 19 scan chains. The table shows both values of TPA and WSA for the top-ranked patterns. It can be seen that both procedures rank the test patterns differently. Especially the highest ranked pattern is different. Experiments on other benchmark circuits (not given here due to page limitation) confirm the differences of both rankings.

In order to validate the TPA ranking, we applied the proposed approach to an industrial design. Figure 5 shows the variation of the calculated TPA and WSA for the industrial design, which has 13114 scan cells arranged in 34 scan chains and total 176230 gates. The test patterns are ordered according to the TPA value. The yellow line shows the TPA value, while the blue line gives the WSA value of the capture cycle. The peaks of the blue line indicate the differences in both pattern ranking schemes. Even in an industrial environment, the accurate simulation of all patterns is not feasible. The run time for a single pattern can last a few days or even a week. The TPA as well as WSA values have been calculated for all generated test patterns. Then, the highest ranked TPA and WSA patterns have been selected for an accurate analysis, i.e. dynamic power and IR-drop analysis.

The capture power cycle of the test patterns has been analyzed in detail using a commercial tool. This took around 1 hour per test pattern depending of the time frame accuracy and step size. The run time of the TPA-based analysis took only about one minute for each test pattern considering all shift cycles and the capture cycle. Therefore, the proposed approach is significantly faster and able to analyze all patterns which makes it suitable for pattern pre-selection.

The results are given in Table IV and V in which patterns are rated according to TPA and WSA. Column *Pattern* gives the pattern id, while columns *Switch_power, TPA*, *WSA* give the results of the corresponding analysis method and columns *SPR, TPAR, WSAR* gives the position in the ranking of the corresponding power metric, i.e. switching power, TPA and WSA. The switching power is the power determined by the accurate commercial tool. The TPA ranking can be better correlated with dynamic switching power than the WSA ranking. It can be seen that the ten highest TPA ranked patterns cover eight of the ten highest switching power patterns. In contrast, the ten highest WSA ranked patterns cover only four of the ten highest switching power patterns.

The results also show that the highest rated WSA pattern, i.e. P_75, actually consumes less power as compared to the highest TPA rated pattern, i.e. P_40. This is similar for other patterns, which are higher ranked but actually consume less power compared to other patterns. Some patterns are equally ranked, e.g. P_4. However, the TPA ranking is also not completely accurate due to its approximation nature, e.g.

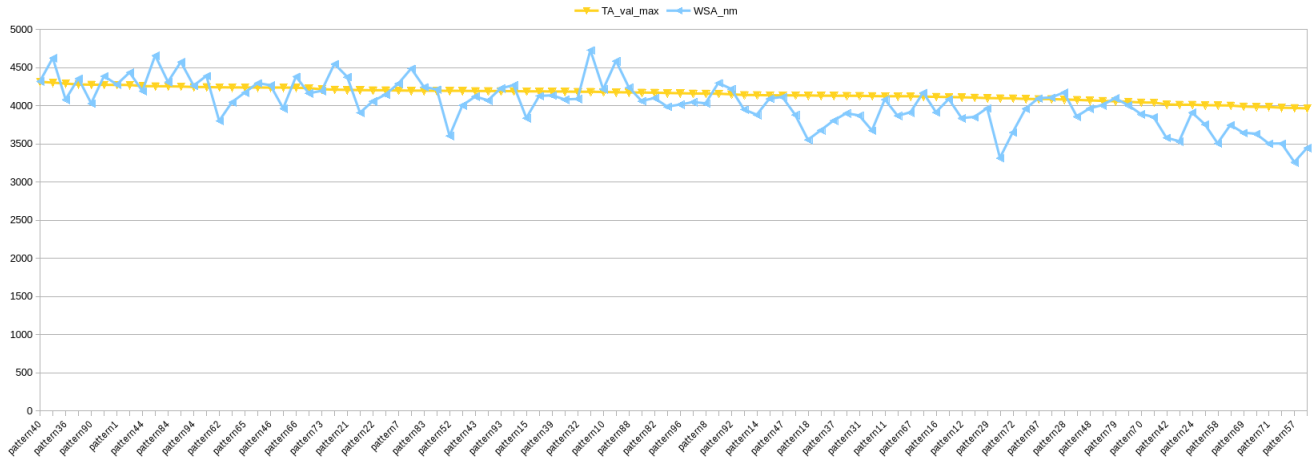

Fig. 5: TPA and WSA rated patterns for industrial design

TABLE IV: TPA rated patterns

Pattern	Switch_power	TPA	WSA	SPR	TPAR	WSAR
P_40	6.1675E-04	4310.49	64,775	9	1	14
P_87	6.4177E-04	4299.67	69,348	3	2	3
P_86	6.4580E-04	4287.05	59,834	2	3	61
P_81	5.7924E-04	4275.38	65,333	14	4	13
P_90	5.8136E-04	4273.21	60,427	12	5	56
P_45	6.6946E-04	4270.56	65,788	1	6	10
P_1	6.2845E-04	4269.62	64,139	6	7	19
P_4	6.3555E-04	4269.19	66,501	4	8	8
P_44	6.3483E-04	4254.17	62,850	5	9	30
P_36	6.2203E-04	4252.88	61,183	8	10	49

TABLE V: WSA rated patterns

Pattern	Switch_power	TPA	WSA	SPR	TPAR	WSAR
P_75	5.6223E-04	4180.03	70,899	15	44	1
P_46	5.6001E-04	4185.89	70,121	16	37	2
P_87	6.4177E-04	4299.67	69,348	3	2	3
P_6	6.0450E-04	4173.86	68,772	10	46	4
P_5	5.8046E-04	4248.38	68,573	13	12	5
P_74	5.9245E-04	4207.91	68,191	11	24	6
P_94	5.4139E-04	4157.30	67,440	17	58	7
P_4	6.3555E-04	4269.19	66,501	4	8	8
P_3	6.2827E-04	4241.87	65,821	7	14	9
P_45	6.6946E-04	4270.56	65,788	1	6	10

leakage power is not considered during the calculations.

In a further experiment, the localization of concentrated power dissipation is analyzed. We analyzed the capture cycle of pattern P_25 using a commercial tool for IR-drop analysis. Figure 6 shows the IR-drop contour of the layout of the industrial design as a result, while Figure 7 shows the TPA cluster map for the same pattern and same cycle. A detailed analysis of the TPA-based clustering has shown that the clusters with the high TPA values correlates with the regions where IR-drop occurs according to the accurate analysis.

Typically, a design-specific threshold (filter) is defined to identify power-critical areas of the design. More than 67% of the instances predicted from the TPA-based clustering approach have been correctly categorized according to the filter. Figure 8 shows the instance based power density map for P_25 obtained from the commercial tool, whereas Figure 9 shows the cluster-based TPA density instances. A detailed analysis of the underlying data has shown that same area and instances are highlighted in both figures, which indicates the similarity of the obtained results.

The experimental results have shown that the method correlates well with the accurate simulation data and is therefore well suited for pattern pre-selection.

VI. Conclusion and Future Work

The accurate power simulation of test patterns is crucial for the sign-off stage of modern circuits. However, the accurate simulation of all patterns is not possible due to excessive run time. Therefore, there is a need for a method to pre-select tests for accurate simulation. We have proposed the *Transient Power Activity* (TPA) metric which takes technology data into account and is used to rank the patterns approximately due to their power dissipation. This method is much faster and, therefore, well suited for a depdendable pattern pre-selection. Since the identification of power-critical areas becomes more and more important, the approach is combined with a machine learning based clustering approach. Here, dynamic clusters of instances with concentrated high switching activity can be identified. Experiments on benchmark circuits and an industrial circuit showed that the proposed metric correlates well with the accurate simulation results of commercial tools. Future work is to consider STA and SPEF information to increase the accuracy. Also the power-grid has to be taken into account.

VII. Acknowledgment

The work has been supported by the Institutional Strategy of the University of Bremen, funded by the German Excellence Initiative and by the German Research Foundation (DFG) under contract number EG 290/5-1.

References

[1] F. Bao, M. Tehranipoor, and H. Chen, "Worst-case critical-path delay analysis considering power-supply noise," in *IEEE Asian Test Symp.*, 2013, pp. 37–42.

[2] A. Chandra and K. Chakrabarty, "Low-power scan testing and test data compression for system-on-a-chip," *IEEE Trans. on CAD of Integr. Circ. and Sys.*, vol. 21, no. 5, pp. 597–604, 2002.

[3] C. W. Chen, J. Luo, and K. J. Parker, "Image segmentation via adaptive K-mean clustering and knowledge-based morphological operations with biomedical applications," *IEEE Transactions on Image Processing*, vol. 7, no. 12, pp. 1673–1683, 1998.

[4] D. A. Clausi, "K-means iterative fisher (kif) unsupervised clustering algorithm applied to image texture segmentation," *Pattern Recognition*, vol. 35, no. 9, pp. 1959–1972, 2002.

[5] V. Devanathan, C. Ravikumar, and V. Kamakoti, "On power-profiling and pattern generation for power-safe scan tests," in *Design, Automation and Test in Europe*, 2007, pp. 1–6.

[6] H. Dhotre, S. Eggersglüß, and R. Drechsler, "Identification of efficient clustering techniques for test power activity on the layout," in *IEEE Asian Test Symp.*, 2017.

[7] S. Eggersglüß, K. Miyase, and X. Wen, "SAT-based post-processing for regional capture power reduction in at-speed scan test generation," in *IEEE European Test Symp.*, 2016, pp. 1–6.

[8] S. Kiamehr, F. Firouzi, and M. B. Tahoori, "A layout-aware X-filling approach for dynamic power supply noise reduction in at-speed scan testing," in *IEEE European Test Symp.*, 2013, pp. 52–57.

[9] J. Lee and M. Tehranipoor, "Layout-aware transition-delay fault pattern generation with evenly distributed switching activity," *Journal of Low Power Electronics*, vol. 4, no. 3, pp. 1–12, 2008.

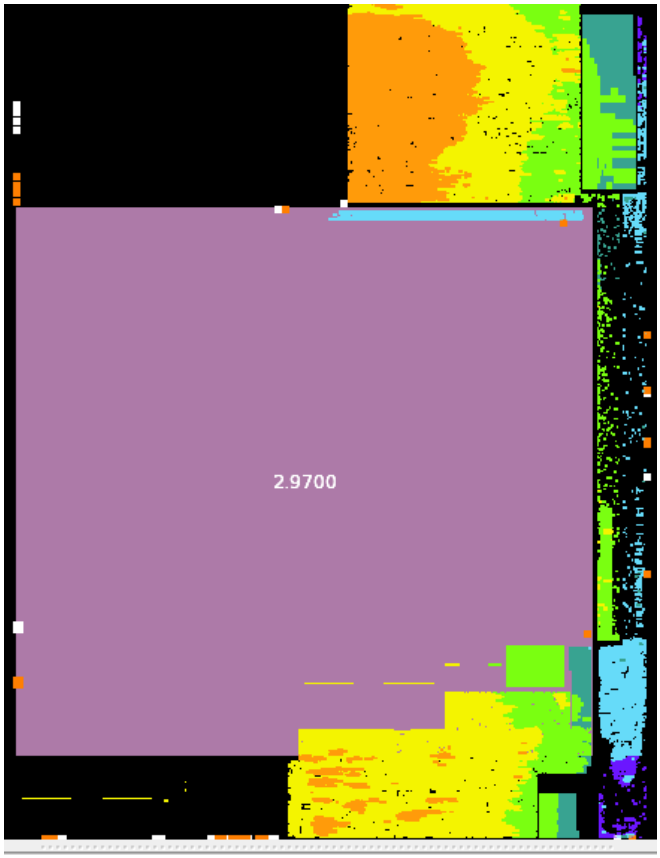

Fig. 6: IR-drop contour of the industrial design

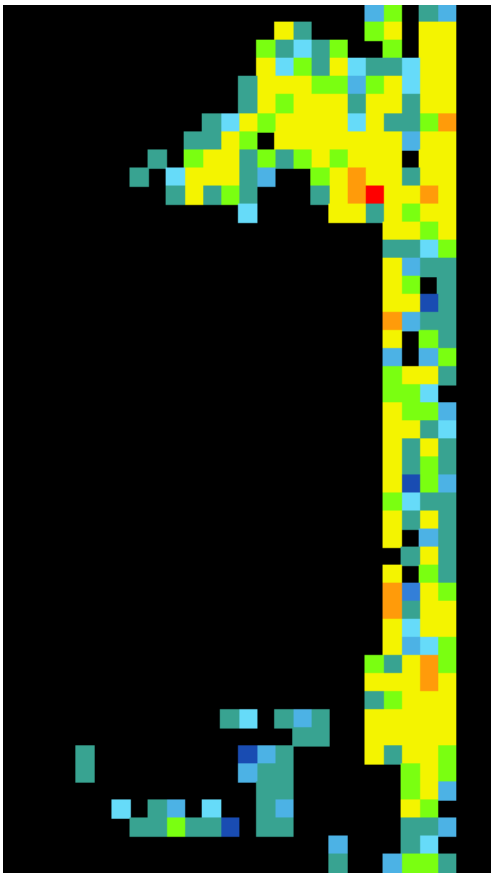

Fig. 8: Power density map of commercial tool

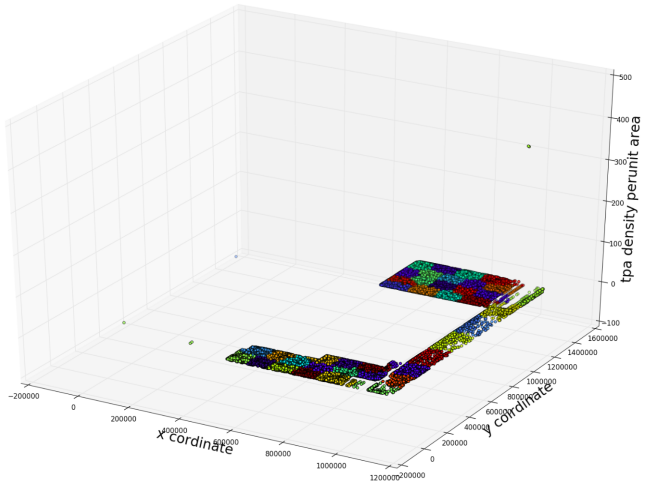

Fig. 7: Clusters of power critical areas of proposed approach

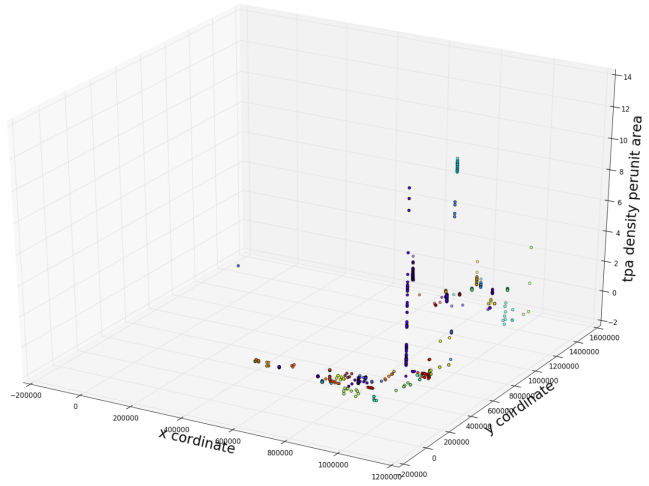

Fig. 9: TPA density map of proposed approach

[10] ——, "Layout-aware transition-delay fault pattern generation with evenly distributed switching activity," *Journal of Low Power Electronics*, vol. 4, no. 3, pp. 360–371, 2008.

[11] Y.-H. Li, W.-C. Lien, C. Lin, and K.-J. Lee, "Capture-power-safe test pattern determination for at-speed scan-based testing," *IEEE Trans. on CAD of Integr. Circ. and Sys.*, vol. 33, no. 1, pp. 127–138, 2014.

[12] J. Ma, M. Tehranipoor, and P. Girard, "A layout-aware pattern grading procedure for critical paths considering power supply noise and crosstalk," *Journal of Electronic Testing: Theory and Applications*, vol. 28, no. 2, pp. 201–214, 2012.

[13] K. Miyase, M. Sauer, B. Becker, X. Wen, and S. Kajihara, "Identification of high power consuming areas with gate type and logic level information," in *IEEE European Test Symp.*, 2015, pp. 1–6.

[14] C. Piguet, *Low-power electronics design*. CRC press, 2004.

[15] H. Sabaghian-Bidgoli, M. Namaki-Shoushtari, and Z. Navabi, "A probabilistic and constraint based approach for low power test generation," in *IEEE Asian Test Symp.*, 2012, pp. 113–118.

[16] M. Sonka, V. Hlavac, and R. Boyle, *Image processing, analysis, and machine vision*. Cengage Learning, 2014.

[17] M.-F. Wu, H.-C. Pan, T.-H. Wang, J.-L. Huang, K.-H. Tsai, and W.-T. Cheng, "Improved weight assignment for logic switching activity during at-speed test pattern generation," in *ASP Design Automation Conf.*, 2010, pp. 493–498.

[18] X. Zhang and K. Roy, "Design and synthesis of low power weighted random pattern generator considering peak power reduction," in *IEEE Int'l Symp. on Defect and Fault Toler. in VLSI Sys.*, 1999, pp. 148–156.

[19] W. Zhao, J. Ma, M. Tehranipoor, and S. Chakravarty, "Power-safe application of transition delay fault patterns considering current limit during wafer test," in *IEEE Asian Test Symp.*, 2010, pp. 301–306.