Impact of NBTI on Increasing the Susceptibility of FinFET to Radiation

Frank Sill Torres[1,2] Hussam Amrouch[3] Jörg Henkel[3] Rolf Drechsler[1,2]
[1]Group of Computer Architecture, University of Bremen, Germany
[2]Cyber Physical Systems, DFKI GmbH, Bremen, Germany
[3]Department of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany
{fsillt, drechsler}@uni-bremen.de {amrouch, henkel}@kit.edu

***Abstract*—This work investigates the interaction between Negative Bias Temperature Instability (NBTI) and radiation effects in 14nm FinFET devices. Due to the complex interaction between traps generated by NBTI and induced charges by strikes of ionizing particles, we opted for a complete physical-based analysis using TCAD mixed-mode simulations. This enables an accurate estimation and then modeling of the duration a circuit requires to recover from a particle strike and, thus, return to correct operation under the effects of NBTI. This a crucial aspect, because the longer the recovery time, the higher the probabilities of a soft-error and that this error remains undetected. Further, our employed setup enables an accurate determination of the critical charge (Q_{crit}), i. e. the minimum collected charge that results into a faulty transition of a circuit's output node. Our investigation reveals that there is indeed a strong relation between NBTI and the time a circuit remains in faulty state. Consequently, detection schemes must be adapted during circuit's operation to take aging into account in order to avoid that errors remain undetected.**

***Index Terms*—NBTI, Aging, Radiation, Soft-Errors, TCAD, FinFET, Reliability**

I. Introduction

NBTI degradation is a dominating reliability issue in p-FinFET technologies, which has a considerable impact on the electrical proprieties of devices (e. g. threshold voltage, carrier mobility, sub-threshold slope, etc.) [1]. Consequences can be a delay increase in circuits [2] and, thus, performance reductions [3], but also an increased vulnerability against parameter variations and/or extrinsic noise, like strikes of high energetic particles [4], [5], [6]. In case of the particle strikes, soft-errors might be generated if sensitive nodes are hit and the energies are sufficient to generate a long lasting transient fault [7], [8]. *Following these observations, this work investigates for the first time the relation between NBTI and radiation in FinFET technologies using a TCAD-based framework.*

Our novel contributions are as follows:

- We model the impact of NBTI on increasing the susceptibility of p-FinFET devices to radiation from physics to circuit level.
- We demonstrate that NBTI-induced defects notably increase the time a circuit needs to recover after a particle strike impeding existing approaches for error detection.
- We show that NBTI-induced defects reduce the level of the transferred particle energy required to generate a transient fault.

The remainder of this work is as follows. Section II discusses the consequences of energetic particle strikes in integrated technologies. The following Section III introduces the implemented simulation environment, while Section IV presents the obtained results. Finally, Section V summarizes and concludes this work.

II. Soft-Errors

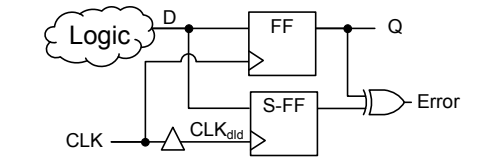
When charged energetic particles strike sensitive transistor nodes, i. e. gate, source and drain contacts, the consequent ionization can lead to a change of the nodes voltage, which might be recognized as glitch at the circuit outputs. In memory or latch circuits this transient signal might result directly into a soft-error (SE), while in combinational logic a transient fault (TF) might be generated [9], [10]. A TF can traverse a circuit and, if not masked by logic, attenuated or vanished before clock signal transition, result into a SE as well. The both latter conditions depend on the time a signal remains faulty. *That means, the longer a transient fault lasts, the higher the probability that it results into a soft-error.* A widely-applied approach for detecting such TF that results into SEs is concurrent error detection based on transition detection, e. g. [11], [12]. The principal idea of these techniques is monitoring the outputs of the actual flipflop (FF) and a shadowed version (S-FF), which receives a delayed clock, and sense erroneous transitions (see Fig. 1). Transition detection profits from reasonable complexity, but its key weakness are long-lasting TFs, which are imperceptible by this approach. *That means, the longer a transient fault lasts, the less the probability that it will be detected as invalid transition.*

III. Simulation Environment

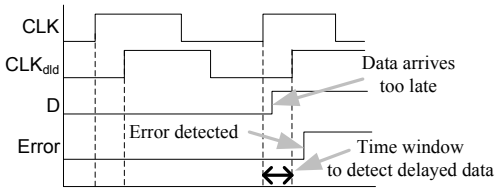
This section introduces how NBTI-induced defects as well as radiation effects are modeled within our implemented TCAD-based framework.

A. TCAD Setup

We employed 14nm p-FinFET and n-FinFET devices TCAD devices based on the available structures provided in [13]

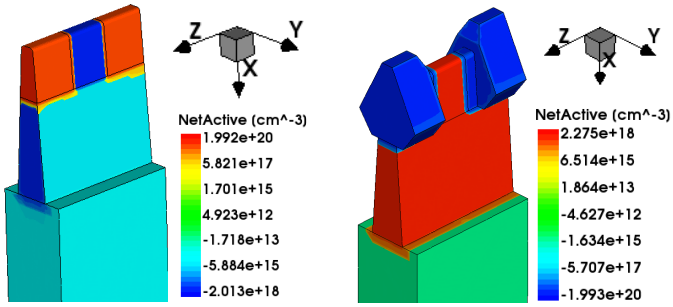


(a) Implementation



(b) Conceptual timing diagram for late arriving input data

Fig. 1: Soft-Error sensing based on transition detection.



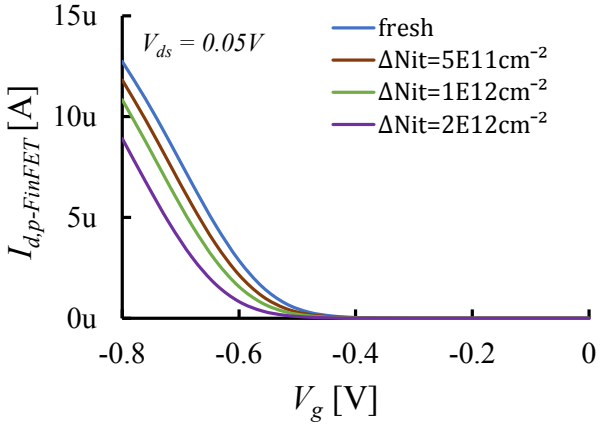
(a) n-FinFET device (b) p-FinFET device

Fig. 2: 3D-views of the doping profiles of the studied 14nm (a) n-FinFET and (b) p-FinFET devices.

for analyzing both NBTI-induced defects and high-energy particles strikes along with the interaction between them (see Fig. 2). However, our work is not limited to a specific FinFET structure and it can be analogously applied to other device structures. The simulated High-k Metal Gate (HKMG) devices consists of tapered fins with rounded corners and height of $h_{fin} = 35$nm and length of $l_{fin} = 25$nm, a dielectric consisting of two monolayers of interlayer SiO_2 (6Å) and HfO_2 (17Å), phosphorus doped SiC S/D junctions (n-FinFET) and Boron *in situ* doped epitaxially grown SiGe S/D junctions (p-FinFET), respectively. Delaunay meshing is used for device simulation with increased mesh densities in the regions of the particle track.

B. Modeling Negative Bias Temperature Instability

NBTI degradation, a dominating reliability issue in p-FinFET technologies, results from the uncorrelated contribution of interface trap generation (ΔN_{it}), trapping in newly generated bulk insulator traps (ΔN_{ot}) and trapping in the pre-existing defects (ΔN_{ht}). In case of well-optimized devices, the impact of pre-existing defects can be ignored [14]. Furthermore, ΔN_{ot} has only under harsh stress conditions a significant contribution to NBTI [15]. That means, for standard



ΔN_{it}	ΔV_T
5E11cm^{-2}	22mV
1E12cm^{-2}	41mV
2E12cm^{-2}	77mV

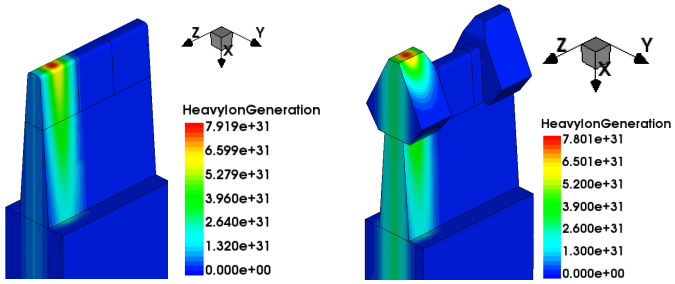
Fig. 3: I_d over V_{gs} for p-FinFET and NBTI-dependent increase of the threshold voltage.

application scenarios the overall NBTI degradation is typically dominated by ΔN_{it}.

Therefore, we modeled NBTI for different ΔN_{it} densities with traps uniformly distributed within the entire bandgap, similar to [1]. The chosen interface trap density values represent different device ages ranging from fresh state ($\Delta N_{it} = 0$), early stages ($\Delta N_{it} = 5e11cm^{-2}$), mid-age ($\Delta N_{it} = 1e12cm^{-2}$) to End-of- Life (EOL) ($\Delta N_{it} = 2e12cm^{-2}$) [1], [2]. The presence of traps results in the reduction of the drain current (I_d) for gate and drain voltages in the transfer and output characteristics of p-FinFET. The consequent increase of the threshold voltage (ΔV_T) was determined for a drain-source voltage (V_{ds}) of 50mV. Fig. 3 depicts the resulting I_d over V_{gs} before (blue line) and after (brown, green, purple lines) incorporating NBTI-induced device degradation represented by different trapped charge concentrations (ΔN_{it}). The extracted shifts of the threshold voltage ΔV_T ranging from $22mV$ up to 77mV (for the induced degradation at EOL) are within reported ranges of similar technologies [15].

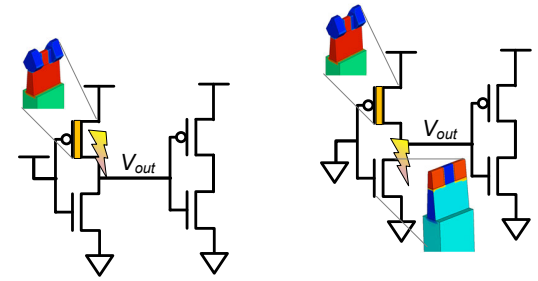
C. Modeling Heavy Ion radiation

Radiation is modeled using a heavy ion model with the particle entering vertically in the center of the drain regions. The ion-track is set to $1\mu m$ length, Gaussian-shaped spatial distribution with characteristic distance of 10nm and linear energy transfer (LET) between 0.4 and $2MeVcm^2mg^{-1}$, which corresponds to low-energy particles like muons and protons which have been reported in [16] as critical for FinFET technologies. The resulting instant heavy ion generation rate of the simulated devices during a high-energy particle strike is depicted in Fig. 4.



(a) n-FinFET (b) p-FinFET

Fig. 4: 3D-views of the instant heavy ion generation rate during a particle strike for both devices.



(a) Configuration 1: Particle strike on p-FinFET (b) Configuration 2: Particle strike on n-FinFET

Fig. 5: Mixed-mode simulation configurations.

D. Mixed-mode simulation configurations

We employed a commercial TCAD tool [13] to perform TCAD mix-mode simulations in order to determine the susceptibility to heavy ion radiation of devices affected by NBTI. Therefore, we implemented two configurations — *configuration 1* for the analysis of the relation between NBTI and heavy ion radiation on the very same device (see Fig. 5a), and *configuration 2* for the analysis of the susceptibility to heavy ion radiation of a circuit whose devices are affected by NBTI (see Fig. 5b). Both configurations apply TCAD models for the devices affected by NBTI and/or radiation (as explained in Section III-B andIII-C, respectively), while the remaining devices are modeled as SPICE elements in order to speed up simulations. These elements are based on the BSIM-CMG model [17] with fin length L_{fin}=25nm and fin height H_{fin}=35nm. The supply voltage is set to V_{DD}=0.8V. Both configurations represent a chain of two inverters, while the second inverter acts as load. We monitored the output voltage (V_{out}) of the first inverter in order to determine the response to a particle strike. Further, we considered the inverter output as faulty if V_{out} crossed $V_{DD}/2$. The impact of NBTI is modeled in both configurations via varying trapped charge concentrations (ΔN_{it}) of the p-FinFET of the first inverter.

In case of *configuration 1*, the input voltage is set to V_{in}=0.8V and the p-FinFET of the first inverter is hit by a heavy ion. The p-FinFET under NBTI and radiation is modeled in TCAD, while the complementary n-FinFET in the inverter configuration and the load devices are modeled in SPICE to reduce the complexity and simulation time (see Fig. 5a). In *configuration 2*, V_{in} is set to 0V and the n-FinFET is hit by a heavy ion. The p-FinFET under NBTI and the hit n-FinFET are modeled in TCAD, while the devices of the load inverter are modeled in SPICE (see Fig. 5b).

IV. Results

This section discusses the obtain results for both implemented configurations.

A. Radiation and NBTI on same FinFET device

We employed *configuration 1* in order to determine the impact of radiation on a device affected by NBTI. The resulting output voltages (V_{out}) of the first inverter and the drain-source current ($I_{d,p-FinFET}$) before (blue lines) and after (brown, green, purple lines) incorporating NBTI-induced device degradation are depicted in Fig. 6.

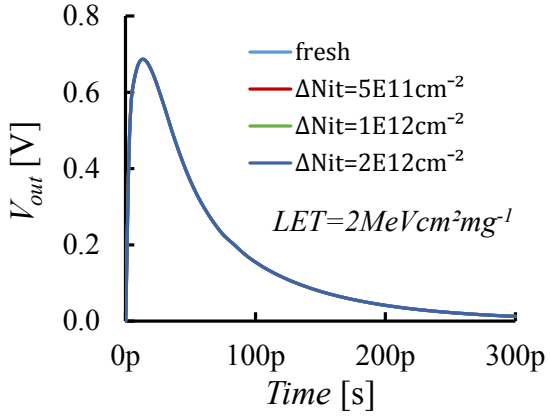
It can be observed that the behavior of V_{out}, which is identical to the drain voltage of the hit p-FinFET, is nearly independent of NBTI (Fig. 6a). The same is valid for the drain current I_d at the affected node (Fig. 6b). The very same observation could be made for lower as well as for relatively high LET levels (depicted in Figs. 6a and 6b).

Thus, it can be concluded that NBTI-induced traps have no impact for devices hit by heavy ions in its drain.

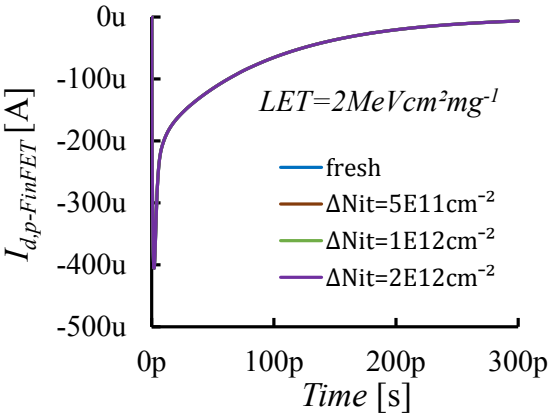
B. Radiation and NBTI on separate FinFET devices

We employed *configuration 2* for the analysis of the impact of NBTI on the circuit response to heavy ion strikes. Therefore, the p-FinFET of the first inverter is aged using varying trapped charge concentrations (ΔN_{it}), while the complementary n-FinFET is hit by heavy ion particles with $LET = 0.6MeVcm^2mg^{-1}$ (see Fig. 7) and $LET = 0.4MeVcm^2mg^{-1}$ (see Fig. 8). Both chosen LET levels are leading to transient faults on the output of the first inverter, i. e. V_{out} crosses $V_{DD}/2$ (gray dashed lines in Figs. 7a and 8a). Further, in a fresh inverter circuit, i. e. without additional trapped charges, a heavy ion strike with $LET = 0.4MeVcm^2mg^{-1}$ leads to the generation of the critical charge (Q_{crit}), which is the minimum charge required to create a transient fault [18]. In case of a heavy ion strike with $LET = 0.6MeVcm^2mg^{-1}$, one can observe a voltage drop of V_{DD} at the output of the fresh inverter circuit.

The response of the inverter output voltage V_{out} for heavy ion strike on n-FinFET with $LET = 0.6MeVcm^2mg^{-1}$ indicates that NBTI is prolonging the duration an inverter remains in faulty state (Fig. 7a). In detail, a fresh inverter recovers within 93ps after entering faulty state to the fault-free state, while the aged versions require additional 13ps ($\Delta N_{it} = 5e11cm^{-2}$), 26ps ($\Delta N_{it} = 1e12cm^{-2}$) and 55ps ($\Delta N_{it} = 2e12cm^{-2}$) at EOL. Further, in the fresh case, V_{out} drops down to 28mV, while degraded versions drop by additional 66mV, 137mV and 283mV. The results for the drain current $I_{d,\text{p-FinFET}}$ of the p-FinFET (Fig. 7d) reveal



(a) Inverter out



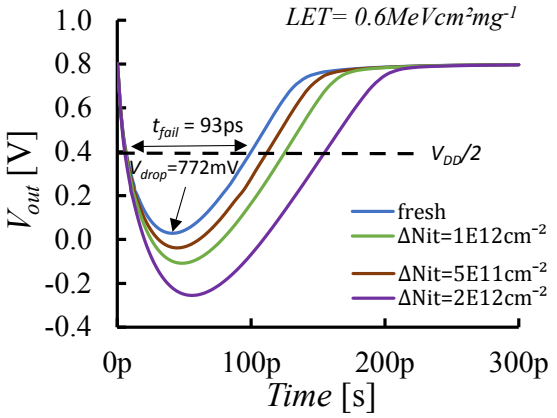
(b) p-FinFET drain current, strike on p-FinFET

Fig. 6: Responses to heavy ion strike with $LET = 2MeVcm^2mg^{-1}$ on p-FinFET before (blue) and after (brown, green, purple) incorporating NBTI-induced device degradation.

the explanation for this prolongation, as the current declines notably with increasing NBTI. In contrast, the drain current $I_{d,\text{n-FinFET}}$ of the n-FinFET device that is hit by the particle is very similar for all aging states of the p-FinFET. The collected charge was estimated with $Q_{coll} = 6.1$fC.

One can conclude that there is an increased probability that the generated transient fault propagates the circuit and turns into a soft-error. Further, the time window for concurrent error detection approaches based on transition sensing is considerably reduced by NBTI. Consequently, there is a higher probability that soft-errors remain undetected.

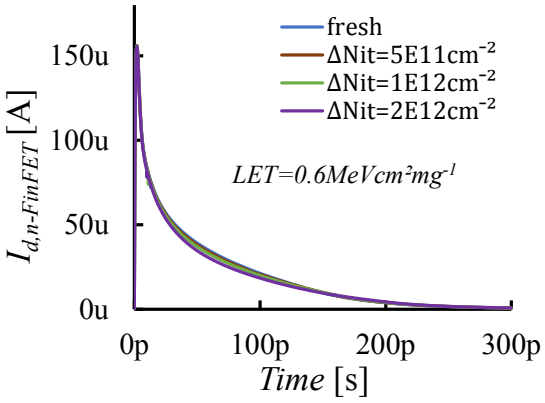
Fig. 8 shows the inverter response V_{out} and drain currents I_d before (blue) and after (brown, green, purple) incorporating NBTI-induced device degradation for heavy ion strike on the n-FinFET of the first inverter with $LET = 0.4MeVcm^2mg^{-1}$. The results are comparable with the previous ones, i. e. the time the circuit is in faulty state depends on NBTI. In detail, the fresh inverter recovers after 12ps from faulty state, while the aged versions require additional 24ps ($\Delta N_{it} = 5e11cm^{-2}$), 42ps ($\Delta N_{it} = 1e12cm^{-2}$) and 76ps



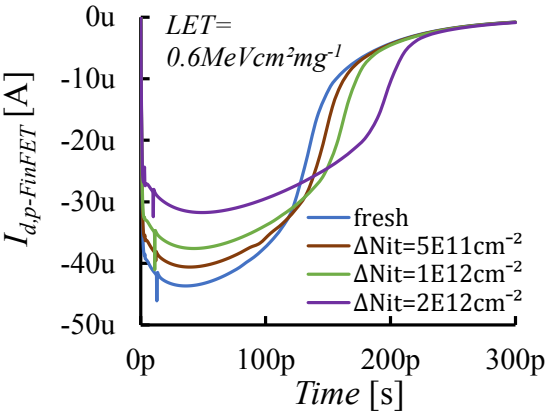
(a) Inverter out

ΔN_{it}	Δt_{fail}	ΔV_{drop}
5E11cm^{-2}	13ps	66mV
1E12cm^{-2}	26ps	137mV
2E12cm^{-2}	55ps	283mV

(b) Measure results



(c) n-FinFET I_d



(d) p-FinFET I_d

Fig. 7: Responses to heavy ion strike with $LET = 0.6MeVcm^2mg^{-1}$ on n-FinFET before (blue) and after (brown, green, purple) incorporating NBTI-induced device degradation.

($\Delta N_{it} = 2e12cm^{-2}$). The collected charge is estimated with $Q_{coll} = 4.2$fC. In the fresh case, V_{out} drops down to 394mV, i. e. nearly $V_{DD}/2$, and thus the charge generated by this LET can be considered as approximately critical charge. In contrast, $Vout$ of the degraded versions drop down by additional 40mV, 68mV and 199mV, meaning that the critical charge is lower in these cases. Again, the drain current ($I_{d,n-FinFET}$) of the n-FinFET, which is hit by the heavy ion, is very similar for all aging states of the p-FinFET. Further, the drain current of the p-FinFET $I_{d,\text{p-FinFET}}$ shows similar relation as above (Fig. 8d).

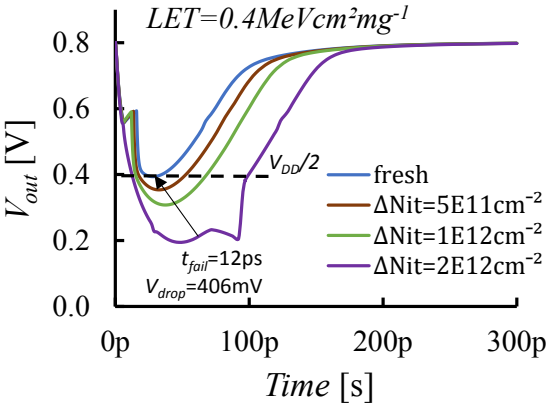
However, one can recognize a spike. Fig. 9 shows a closer view at this disturbance, i. e. a detailed view of the p-FinFET drain current $I_{d,\text{p-FinFET}}$ and the voltage difference $(V_{ds} - V_{gs})$, which is identical to V_{out}. $I_{d,\text{p-FinFET}}$ turns to be constant as the p-FinFET enters saturation remains in this state until the charge accumulation (not shown) at the drain of the n-FinFET increases V_{sd} of p-FinFET leading to increasing absolute currents $I_{d,\text{p-FinFET}}$.

Also these results clearly indicate that *The time a circuit remains in faulty state can be notably increased by NBTI*. Consequently, there is a higher probability that the fault traverses the circuit and turns into a soft-error. Further, the reduction of time window for error monitoring via transition detection increases the chance of undetected soft-errors. Finally, *NBTI reduces the critical charge of a circuit*, confirming results of studies on circuit level, i. e. without TCAD analysis [19].

C. Heavy ion strike response modeling under NBTI effects

Based on the acquired simulation data, we extracted a model for the relation between NBTI-induced increase of the threshold voltage ΔV_T and the circuit response to a heavy ion strike on the n-FinFET drain in a minimum sized inverter (Fig. 10). The circuit response is represented as the extension of time the circuit output remains faulty Δt_{fail} as well as the increase of V_{drop} after the strike. As mentioned in Section III-B, the trapped charge concentrations (ΔN_{it}) have been chosen to represent the device conditions starting from fresh state to end of life (EOL) state and, thus, cover the whole lifetime. Furthermore, the chosen LET level represent the required energy transfer for generating in a fresh device the critical charge ($LET = 0.4MeVcm^2mg^{-1}$) as well as a voltage drop of V_{DD} ($LET = 0.6MeVcm^2mg^{-1}$).

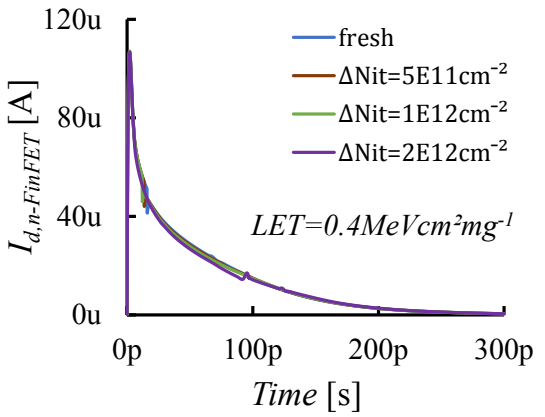
Results indicate for $LET = 0.6MeVcm^2mg^{-1}$ that in early stages the voltage drop V_{drop} increases by 9%, while the time in faulty state t_{fail} increases by 13% compared to the fresh state. In mid-age stages, V_{drop} increases by 18% and t_{fail} by 28%, while at EOL V_{drop} is 37% higher and t_{fail} is 37% longer. In case of $LET = 0.6MeVcm^2mg^{-1}$, V_{drop} increases by 10% and t_{fail} by factor 2 in early stages. In mid-age stages, V_{drop} increases by 21% and t_{fail} by factor 3.5, while at EOL V_{drop} is 49% higher and t_{fail} is by factor 6.5 longer. Please note that the strong increase of t_{fail} results from the nearly zero fault time in fresh state.



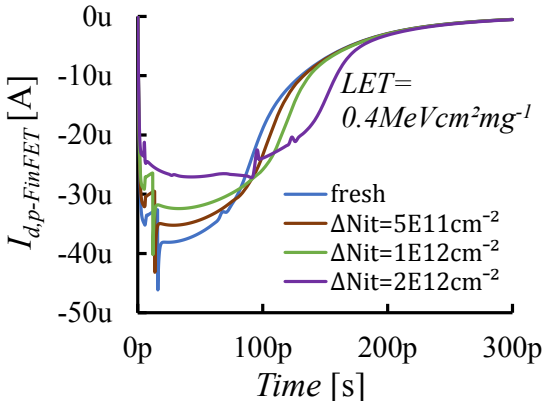
(a) Inverter out, strike on n-FinFET

ΔN_{it}	Δt_{fail}	ΔV_{drop}
5E11cm^{-2}	24ps	40mV
1E12cm^{-2}	42ps	86mV
2E12cm^{-2}	76ps	199mV

(b) Measure results



(c) n-FinFET I_d, strike on n-FinFET



(d) p-FinFET I_d, strike on n-FinFET

Fig. 8: Responses to heavy ion strike with $LET = 0.4MeVcm^2mg^{-1}$ on n-FinFET before (blue) and after (brown, green, purple) incorporating NBTI-induced device degradation.

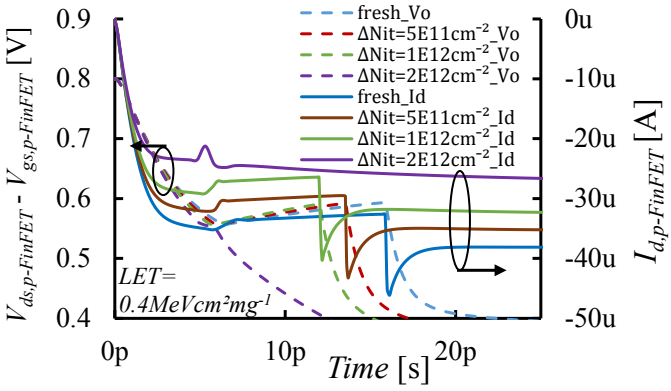


Fig. 9: p-FinFET I_d and $V_{ds} - V_{gs}$ after heavy ion strike with $LET = 0.4MeVcm^2mg^{-1}$ on n-FinFET before (blue) and after (brown, green, purple) incorporating NBTI-induced device degradation.

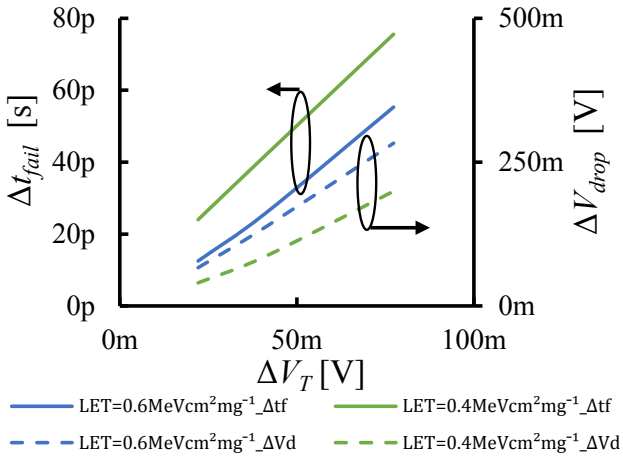


Fig. 10: Model for circuit response to heavy ion strike under NBTI effects.

V. Conclusions

We investigated in this work the impact of NBTI on the increasing susceptibility of p-FinFET to radiation from physics to circuits. We showed that NBTI reduces the critical charge levels required for generating transient faults. Furthermore, results revealed that NBTI notably increases the time circuits remain within faulty state after strike of ionizing particles. This prolongation increases the probability that a radiation induced transient fault turns into a soft-error and that a soft-error remains undetected for widely-applied concurrent error detection schemes.

Acknowledgments

The authors would like to thank Souvik Mahapatra and his team for the valuable support regarding NBTI modeling.

References

[1] S. Mishra, H. Amrouch, J. Joe, C. K. Dabhi, K. Thakor *et al.*, "A simulation study of nbti impact on 14-nm node finfet technology for logic applications: Device degradation to circuit-level interaction," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 271–278, 2019.

[2] A. Thirunavukkarasu, H. Amrouch, J. Joe, N. Goel, N. Parihar *et al.*, "Device to circuit framework for activity-dependent nbti aging in digital circuits," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 316–323, 2019.

[3] H. Amrouch, B. Khaleghi, A. Gerstlauer, and J. Henkel, "Reliability-aware design to suppress aging," in *Design Device to Circuit Conference (DAC)*. ACM, 2016, pp. 12:1–12:6.

[4] J. Autran and D. Munteanu, *Soft Errors: From Particles to Circuits*, ser. Devices, circuits, and systems. CRC Press, 2015.

[5] R. de Oliveira Rocha, F. Sill Torres, and R. Possamai Bastos, "Towards high-sensitive built-in current sensors enabling detection of radiation-induced soft errors," *Microelectronics Reliability*, vol. 78, pp. 190 – 196, 2017.

[6] H. Amrouch, V. M. van Santen, T. Ebi, V. Wenzel, and J. Henkel, "Towards interdependencies of aging mechanisms," in *Proceedings of the 2014 IEEE/ACM International Conference on Computer-Aided Design*. IEEE Press, 2014, pp. 478–485.

[7] E. H. Cannon, A. KleinOsowski, R. Kanj, D. D. Reinhardt, and R. V. Joshi, "The impact of aging effects and manufacturing variation on sram soft-error rate," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 1, pp. 145–152, March 2008.

[8] M. Bagatin, S. Gerardin, A. Paccagnella, and F. Faccio, "Impact of nbti aging on the single-event upset of sram cells," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3245–3250, Dec 2010.

[9] T. Uemura, S. Lee, J. Park, S. Pae, and H. Lee, "Investigation of logic circuit soft error rate (ser) in 14nm finfet technology," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, April 2016, pp. 3B–4–1–3B–4–4.

[10] J. G. Melo and F. Sill Torres, "Exploration of noise impact on integrated bulk current sensors," *J. Electron. Test.*, vol. 32, no. 2, pp. 163–173, Apr. 2016.

[11] K. A. Bowman, J. W. Tschanz, N. S. Kim, J. C. Lee, C. B. Wilkerson *et al.*, "Energy-efficient and metastability-immune resilient circuits for dynamic variation tolerance," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 49–63, Jan 2009.

[12] A. Silva and F. Sill, "Mitigation of aging effects through selective time-borrowing and alternative path activation," in *2017 30th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug 2017, pp. 210–216.

[13] Synopsys, "Sentaurus TCAD," 2017.

[14] N. Parihar, R. G. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "Modeling of nbti kinetics in rmg si and sige finfets, part-i: Dc stress and recovery," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 1699–1706, May 2018.

[15] N. Parihar, R. Southwick, M. Wang, J. H. Stathis, and S. Mahapatra, "Modeling of nbti time kinetics and t dependence of vaf in sige p-finfets," in *IEEE International Electron Devices Meeting (IEDM)*, Dec 2017, pp. 7.3.1–7.3.4.

[16] G. Hubert, L. Artola, and D. Regis, "Impact of scaling on the soft error sensitivity of bulk, FDSOI and finfet technologies due to atmospheric radiation," *Integration*, vol. 50, pp. 39–47, 2015.

[17] Y. Chauhan, D. Lu, V. Sriramkumar, S. Khandelwal, J. Duarte *et al.*, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. Elsevier Science, 2015.

[18] M. Sajid, N. Chechenin, F. S. Torres, M. N. Hanif, U. A. Gulzari *et al.*, "Analysis of total ionizing dose effects for highly scaled cmos devices in low earth orbit," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 428, pp. 30 – 37, 2018.

[19] D. Rossi, M. Omaña, C. Metra, and A. Paccagnella, "Impact of bias temperature instability on soft error susceptibility," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 4, pp. 743–751, April 2015.