RC-IJTAG: A Methodology for Designing Remotely-Controlled IEEE 1687 Scan Networks

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***Abstract*—Incorporating effective scan infrastructures is becoming increasingly necessary due to the growing complexity of modern system-on-chips, as it provides efficient access to embedded instruments. IEEE 1687 Std. (IJTAG) addresses this fundamental requirement by introducing a reconfigurable access methodology which contributes to reducing the overall access time. This is achieved by integrating programmable elements into the network to shorten the length of the scan chain. However, the additional time overhead due to the configuration of these components poses a significant challenge to the IJTAG networks. This work tackles the problem by proposing a methodology for designing remotely controlled multi-power domain IJTAG networks based on prior knowledge about the instrument access plan and the power characteristics of the circuit. More precisely, the proposed methodology describes how to synthesize an IJTAG network to avoid unnecessary data shifting through the configuration registers to finally minimize the overall access time. This approach results in designing an instrument scan network that is controlled remotely through another reconfigurable network. The experimental results prove a considerable reduction of the overall access time and area overhead compared to the benchmark networks.**

I. Introduction

The test time is considered as one of the main factors contributing to the final cost in the commercial semiconductor industry. Accordingly, long scan paths, which result in higher access time in modern *System-On-Chips* (SoCs), is being viewed as a major bottleneck in SoC design and manufacturing. IEEE 1687 Std. (IJTAG) has introduced an efficient technique to cope with the challenge of long scan chains while accessing the embedded instruments in the state-of-the-art SoCs [1]. Programmable elements like *ScanMux Control Bits* (SCBs) and *Scan Insertion Bits* (SIBs) enable the reconfiguration of the IJTAG scan networks to set up shorter scan chains. This is achieved by excluding the parts of the scan network that are not required to be accessed in the current access session. According to the latest chip design paradigms, SOCs can be partitioned into several power domains to manage the workload [2] better. Every domain has a power constraint that limits the number of instruments that can be concurrently accessed over an access session. Since the test process starts after the end of the design phase, the instruments' power consumption and their required access patterns are provided as given constraints [3]. Based on this information, test schedulers are able to calculate an optimized access sequence to the instruments that minimizes the overall test time [4]–[6].

However, introducing the programmable elements itself incurs some access time overhead [7]. During the manufacturing test, the time spent on each fabricated circuit impacts the total cost [3]. Significant research has been carried out that addresses the access time challenge in reconfigurable scan networks [4]–[19]. A method for the access time analysis is presented in [7]. Design automation for reconfigurable scan networks is discussed in [8], [20]. Some network retargeting techniques are proposed in [9]–[12] to improve the instrument access time without applying any structural modifications to the network. In [13], [19], [21], the authors have exploited the Boolean satisfiability problem to optimize the instrument access time for scan pattern retargeting in reconfigurable scan networks that do not include SIBs. Test scheduling under resource and power constraints is described in [14], [22]. A hybrid scheduling technique is presented in [14] to create a purely SIB-based network with minimized SIB programming overhead. Authors in [4]–[6] have proposed methods for optimization of test scheduling for multi-power domain scan networks. Hardware modification has been another approach for access time reduction. For example, a new SIB structure is proposed in [23] in order to increase the bandwidth of the IJTAG network. This idea is extended in [15] to reduce the test time by sending identical data to the replicated cores using broadcasting techniques. However, these works either are not applicable to multi-power domain networks or do not optimize the network's topology to achieve improved accessibility. Furthermore, some other works like [8], [14] are only applicable to SIB-based networks. In addition, these methods still suffer from time overhead due to the inclusion of programming elements on the scan chain during every read and write from and to the instruments.

This paper introduces a methodology for re-synthesizing the multi-power domain scan networks based on given power and access constraints in the form of *Remotely-Controlled* IJTAG (RC-IJTAG) networks. The proposed method significantly reduces the overall access time overhead by improving the structure of a given IJTAG network. This is accomplished through a new configuration mechanism that does not affect the instruments' initial accessibility. The developed framework exploits remotely programmable elements to finally design a configuration sub-network that controls the scanMuxes of the main instrument scan network. In other words, the final design

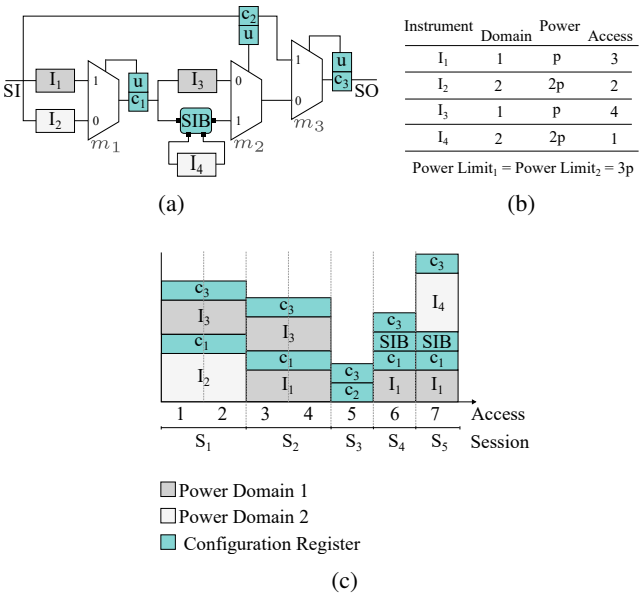
constitutes a *Reconfigurable Scan Network* (RSN) that controls an IJTAG network. Instead of SCBs, new cells are used that enable switching between two different hardware routing in the configuration network. This provides flexibility for possible future changes in the instrument access plan.

The remainder of this paper is organized as follows: Section II provides a background about the access mechanism in IJTAG and the principle of access scheduling in scan networks. The proposed methodology is described in Section 2. The experimental results and evaluation of the proposed method are discussed in Section IV, and, finally, the paper is concluded in Section V.

II. Background

This section gives an overview of the IJTAG networks and briefly introduces the instrument access schedule. Fig. 1a shows an example of a small IJTAG network that provides access to the instruments I_1 to I_4 using one SIB and three SCBs as programmable elements. SIB operates as a switch that can include or exclude I_4. Generally, SIBs can activate a sub-network that is connected to their host ports. SCBs consist of two flip-flops, one is placed on the scan path enabling the shift of data, and the other saves the configuration upon an update signal from the controller. These flip-flops are labeled as c_1-c_3 and u in Fig. 1a, respectively. The in-line SCBs controlling m_1 and m_3 share the same scan path as their multiplexers. The multiplexer m_2 is remotely controlled since no scan chain includes m_2 and its SCB on the same access session. IJTAG networks can be considered as multiplexer-based networks since SIBs can be modeled by scan multiplexers that are controlled by in-line SCBs [4]. The instruments in Fig. 1a are powered by two separate power domains, which are highlighted in different shades. The sum of the power consumption of concurrently active instruments (in one power domain) should not violate the domain's power constraint. Every access to the instruments of the active scan chain is provided during a *Capture-Shift-Update* (CSU) cycle. The instruments are connected to the network using *Test Data Registers* (TDR), which provide both serial and parallel data transfer. The data is shifted serially from *Scan-In* (SI) to the *Scan-Out* (SO) port through the active chain over the shift operation while transferring the data between TDRs and instruments is done concurrently by asserting the capture or update signals from a controller. CSUs containing exactly the same instruments are called an access session.

The IJTAG network in Fig. 1a allows for the creation of seven different paths between SI and SO, which yields six combinations of instruments, namely $\{(I_1, I_3), (I_1, I_4), (I_2, I_3), (I_2, I_4), (I_1), (I_2)\}$. Assuming $\{a_1 = 3, a_2 = 2, a_3 = 4, a_4 = 1\}$ as the required number of accesses to the instruments I_1 to I_4, Fig. 1c shows a valid access schedule for Fig. 1a. According to the data given in Fig. 1b, the concurrent activation of I_2 and I_4 exceeds the power limit, and, hence, the schedule cannot include a session containing both instruments. The schedule in Fig. 1c requires seven CSUs over five sessions to fulfill all required accesses. Session one includes two CSUs over which one scan chain is



Instrument	Domain	Power	Access
I_1	1	p	3
I_2	2	2p	2
I_3	1	p	4
I_4	2	2p	1

Power Limit$_1$ = Power Limit$_2$ = 3p

Fig. 1: (a) A small IJTAG network with two power domains that provides access to instruments I_1-I_4 (b) The power constraints and access requirements (c) The corresponding access schedule for the network (a) based on the given constraints.

configured to transfer two sets of data to the instruments I_2 and I_3 concurrently.

The advantage of IJTAG over the legacy access approaches is excluding the redundant segments of the design in every session and, hence, shortening the active scan chain, which yields lower test costs. However, in-line configuration registers inevitably cause time overhead during the shift phase in the instrument access session. For example, the active chain in the first session of Fig. 1c includes c_1 and c_3 and therefore, every access to I_2 and I_3 in this session requires two extra clock cycles. Despite remote configuration time that is not affected by the number of access to the instruments, the time overhead due to in-line registers rises considerably by increasing the number of test patterns in larger circuits.

III. Proposed Configuration Methodology

This session proposes a methodology to minimize the time overhead due to in-line configuration registers by resynthesizing an IJTAG network and developing a new structure for the network reconfiguration mechanism. In an access schedule with n_s CSUs and c_s in-line SCBs in session s, the overall time overhead due to in-line configuration bits would be $\sum_{s \in S}(n_s \cdot c_s)$, where S indicates the set of access sessions. For example, every access to the instruments in Fig. 1a requires at least two extra clock cycles to shift the data through c_1 and c_3, causing an overall time overhead of 12 clock cycles over six accesses, as exemplary given in Fig. 1c. Exploiting multiplexers in IJTAG networks to shorten the scan paths, results in the creation of parallel branches, which cannot be activated concurrently over an access session. Consequently, IJTAG limits the possible combination of instruments for concurrent access in order to improve the timing feature. For example, in Fig. 1a, the instruments I_1 and I_2 cannot be accessed through a common

scan chain. Accordingly, in order to prevent future restrictions on instrument concurrent accessibility, prior knowledge about the instrument access plan should be provided before incorporating the scan network. The proposed method uses this already available information to design an optimized network with improved overall access time. The main idea is about preventing the data of the instruments from shifting through the configuration registers during the instrument access phase and, consequently, limiting the contribution of these registers only to the configuration step. Since the proposed approach considers the same constraints and access requirements of the original IJTAG network, no further access restrictions are imposed on the synthesized network.

Basically, the proposed method divides the IJTAG network into four main segments.

1) The first part is the *Instrument Scan Network* (ISN) that is obtained by removing the configuration registers from the original IJTAG network and includes only the instruments and multiplexers.
2) The second segment is another IJTAG network composed of configuration cells controlling the multiplexers of the ISN.
3) The third segment is a branch of solely programmable registers that selects the required chain for the network's configuration.
4) Finally, the last block controls the activation of the previous segments to realize the intended instrument access plan.

The design process is divided into three main phases that are explained in the following subsections.

A. Network Analysis

In the first step, the given network is analyzed to obtain the required information for later optimization and synthesis. The structure of the IJTAG network, which is described by the *Instrument Connectivity Language* (ICL) is modeled as a directed acyclic graph [4], [24]. Based on the method introduced in [5], [21], a Boolean definition of the network in *Conjunctive Normal Form* (CNF) is created. This Boolean expression is subsequently used to define the structural constraint of the network. The CNF representation defines all potential scan chains between SI and SO. The structural constraint guarantees that at least one valid scan chain exists in the network over which the scheduled instruments can be accessed in a session concurrently. The network analysis and modeling enable the scheduling of instruments' access as an initial optimization is performed only via shifting an optimized data sequence through the network. Along with structural, power, access, and security constraints are used to calculate the optimized schedule [6]. Instruments' access constraints define the number of patterns required to test an instrument. Furthermore, bound access to several instruments can be added to the optimization problem as another non-functional property. Further constraints concerning the power consumption and the power domain partitioning ensure that the scheduled instruments do not violate the domain's power limit. Any other intended combination of instruments, such as secure exclusive access, can also be considered to create a final access plan.

B. Configuration Network Design

In order to design the configuration network, the active ScanMuxes in every session of the access plan should be extracted. For this, the CNF of the network is solved for every session while the scheduled instruments are set to $True$. The satisfying model of the propositional formula includes all required ScanMuxes for configuring the corresponding scan chain. Since every ScanMux needs a control register, the registers required to configure every session are consequently determined. Given the set of configuration registers for every session, the developed framework connects these nodes to create a chain sourcing from SI and sinking to SO. Subsequently, these configuration chains are combined to generate a directed acyclic graph. For example, in Fig. 1a, the set of all possible configuration paths for implementing the intended schedule is $\{[SI, c_2, c_3, SO], [SI, c_1, c_3, SO], [SI, c_1, SIB, c_3, SO]\}$. This set can define different directed acyclic graphs of configuration elements. Since different chains potentially share some of the registers, the final graph resulting from combining these chains can contain merging nodes implying the synthesis of multiplexers. As the configuration sets do not define a unique graph, changing the sequence of nodes on every chain leads to different graphs with different numbers of generated multiplexers. Thus, a heuristic algorithm is applied to create a network with minimum number of multiplexers. This optimization allows for reducing the number of control bits that are required to control the generated multiplexers. The framework sorts the nodes based on the number of times they appear in different sessions and the nodes with higher sharing degrees are given priority for joining the graph. The already created paths are used in later chains to avoid unnecessary routing overhead. Furthermore, following the IEEE 1687 Std. network design guideline, it should be noted that no cycles are created in the graph construction process since this is considered a bad design practice. Essentially, the incremental procedure of combining the configuration chains creates a new IJTAG network that consists of programmable elements and is used as a remote configuration block for controlling the ISN block. Every chain of the *Remote Configuration Network* (RCN) activates one chain of the ISN and establishes an access session accordingly. The control registers of the multiplexers that are generated during the graph construction are implemented serially on a remote chain called *Configuration Selection*. This prevents a time overhead while shifting the configuration vectors through the RCN block. Despite SCBs which contain two flip-flops for shift and update operations, these selector cells do not need an update flip-flop and are implemented by single registers. Fig. 2a shows an example of the proposed remote configuration architecture for a hypothetical instrument scan network with eight multiplexers. Eight inline SCBs controlling these multiplexers are implemented as a remote configuration network with eight single-bit configuration registers and three multiplexers. The figure does not show clock and control signals for a more comprehensive representation. As is shown in Fig. 2b, the remote

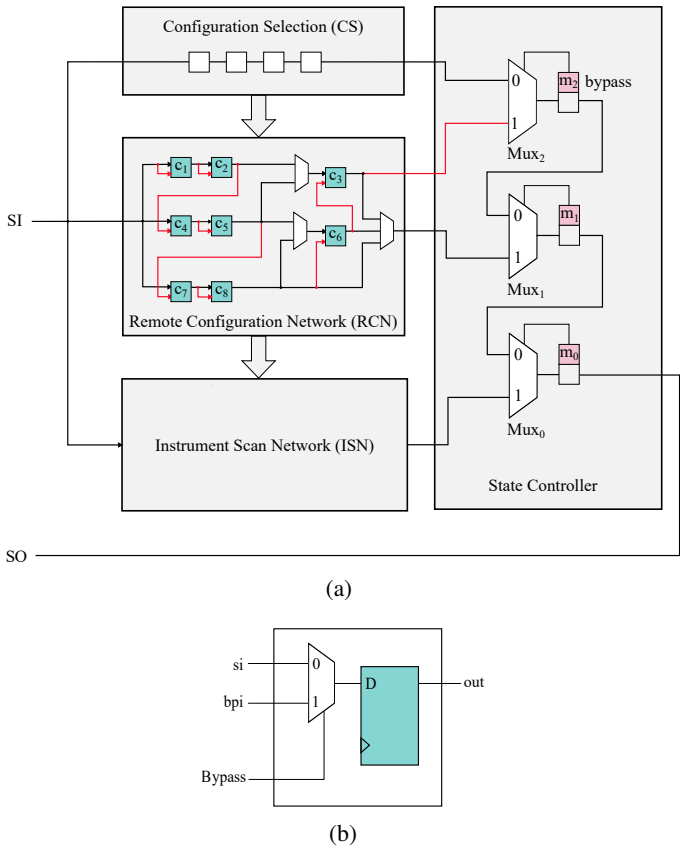


Fig. 2: (a) Proposed remote configuration architecture for an instrument scan network with eight multiplexers (b) Configuration cell with Bypass input used in the RCN block

configuration cells have an extra *bypass input* (bpi) that enables an alternative routing strategy for the same elements. The bypass port of all configuration cells in the remote configuration block is connected to the mode selection bit m_2. By asserting the bypass signal, the configuration network transforms into a serial chain, including all configuration cells. Although the designed network is tailored for an optimized access to the instruments, providing a bypass path enables future arbitrary changes regarding the access scenarios. Furthermore, another advantage of this alternative chain is the capability of accessing all configuration registers over one CSU, which provides even more flexibility in controlling the ScanMuxes of an ISN segment compared n to the original IJTAG network architecture. However, exploiting this extra feature in bypass mode requires shifting a longer configuration pattern into the bypass chain. Nevertheless, the proposed configuration cell still allows for designing a desired alternative network instead of the daisy bypass chain when required. Some control bits can be excluded from the bypass chain according to design requirements, such as exclusive instrument access, which needs a dedicated path between SI and SO that can be configured using only one multiplexer.

C. State Controller

After designing the remote configuration block and the selectors chain, all configuration registers are removed from the

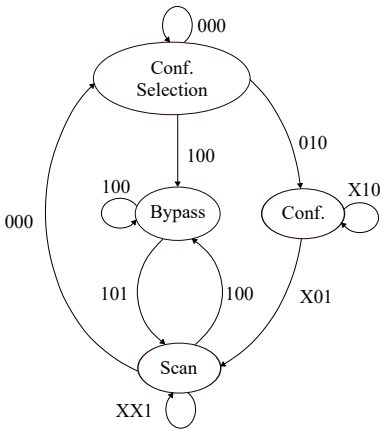


Fig. 3: Control states of proposed remote configuration architecture with state control registers [m_2, m_1, m_0] as input. Don't care bits are represented by X.

original IJTAG network. Subsequently, the select inputs of the internal multiplexers of SIBs and ScanMuxes are rerouted to the corresponding programmable cells in the remote network. In order to control the sequence of activation of the three main blocks of the synthesized network, a state controller is designed, which uses the same control signals issued by the network's TAP controller. As is shown in Fig. 2a, the state controller consists of three multiplexers Mux_2, Mux_1 and Mux_0 which enable the selection between three operation modes: configuration selection, remote configuration, and instrument scan. The conventional two-flip-flop inline SCBs are used to control these multiplexers through m_2, m_1, and m_0, which are the update flip-flops connected to their select inputs.

At the initial state, all mode selection SCBs are set to 0 and, hence, the *Configuration Selection* branch is active while the other two blocks are excluded from the circuit. The first shift operation is performed over one CSU to program the configuration selection chain. This sets up a path in RCN by configuring the multiplexers of this block. However, as the RCN block is not activated at this stage, the established chain does not contain any patterns yet. During the first CSU, three extra bits $[0, 1, 0]$ are appended to the data being shifted through the configuration selection branch to prepare Mux_2, Mux_1, and Mux_0 for the next step and, consequently, activate the RCN block. Issuing an update signal from the TAP controller induces a switch of the circuit to the remote configuration mode. Subsequently, the required pattern for controlling the ScanMuxes of ISN is shifted through the already created remote configuration chain. Mux_2 is excluded in this mode and only two extra bits $[1, 0]$ are required to be appended to this data to program m_1 and m_0. This prepares the circuit for switching to the next mode. An update signal from the IJTAG controller activates the ISN segment and excludes the other two blocks. This enables the shift of the instrument access data or test patterns through the instruments. In this phase, which includes the highest number of test patterns and shift operations, the configuration circuitry is excluded and does not contribute to the time overhead, except for one extra bit of Mux_0 which should be appended to the input pattern. Since Mux_2 and Mux_1 are already set to 0, assigning 0

to Mux_0 at the end of every instrument access session resets the whole system to the configuration selection mode for starting the next session. In order to activate the bypass mode for the next session, it is sufficient to set m_2 to 1 in the current session during the configuration selection mode. In the case of successive sessions in bypass mode, the circuit does not enter the configuration selection mode and switches only between RCN and ISN blocks. Fig. 3 illustrates the state diagram of the circuit, which includes four states. The *Conf. Selection*, *Conf.*, and *Scan* states are related to the CS, RSN, and ISN blocks, respectively. The transitions are made using the values assigned to m_2, m_1, and m_0 over the update phase of the CSU cycle. It should be noted that not all control inputs are accessible in all states, and, hence, the transitions in such cases depend on the values already assigned in previous cycles. For example, in the *Scan* state only m_0 is accessible. When 0 is assigned to this register, moving to the *bypass* or *Conf. Selection* states depends on the value previously saved in m_2. Among the integrated programmable cells only the registers inside the *State Controller* are comprised of two flip-flops. The flip-flops of these cells use the control signals from the TAP controller to change the operation mode. Therefore, the *State Controller* is compatible with the main IJTAG controller. The programmable cells of RSN and CS blocks are implemented by one flip-flop, and, hence, the proposed method does not incur considerable area overhead in comparison to the original network. Since the incoming patternx from SI is distributed to three blocks, clock gating is used to prevent unnecessary switching in the programmable registers of the blocks that are not included in the active chain. This routing is not shown in Fig. 2a for the sake of visibility. In the end, the introduced architecture provides a *Remotely-Controlled IJTAG* (RC-IJTAG) network that neither sacrifices the instrument accessibility nor causes considerable hardware overhead and is efficient in terms of timing performance.

IV. Experimental Results

In order to evaluate the efficiency of the proposed method, a framework has been developed in C++. All experiments are applied to the ITC'16 IJTAG benchmark set [25] and are carried out on a machine holding an AMD Ryzen 7 Pro 4750U processor and 16GB of main memory. Characteristics of the benchmark networks are presented in Table I. The names of the networks are listed in column (1). Other columns show the number of instruments, SIBs, ScanMuxes, and SCBs in every network, respectively. Applying the RC-IJTAG design methodology on a benchmark with a wide range of instruments from 5 to 1,629 proves the scalability of the proposed method

Table II compares the time and area overhead of the synthesized networks with the benchmark networks. The experiments include the networks with different sizes whose names are listed in column (1). The networks are divided into different power domains, as shown in column (2). For every network, a scheduling scenario is designed by assigning random power consumption and access to the instruments. The sum of instruments' accesses are given in column (3). After calculating the optimized access sequence, the scan chains are extracted

TABLE I: ITC'16 benchmark network characteristics [25]

(1) **Network**	(2) **#Instruments**	(3) **#SIBs**	(4) **#ScanMuxes**	(5) **#SCBs**
Mingle	8	10	13	3
BasicSB	5	-	10	10
TreeFlat	11	12	24	1
TrapOrFlap	12	11	18	7
q12710	23	25	25	-
a586710	22	-	47	47
t512505	128	160	160	-
p22810	242	283	283	-
p34392	73	-	142	142
p93791	550	-	653	653
N17D3	27	7	8	-
N32D6	44	13	10	-
N73D14	90	29	17	-
N132D4	172	39	40	-
NE600P150	793	207	194	-
NE1200P430	1,629	381	430	-

and the number of required CSUs are obtained, as presented in column (4). Every CSU includes several shift operations whose number is determined by the scheduler. Next, the overall clock cycles required to cover all instruments are calculated for both benchmark and generated networks. For this, all instruments are assumed to have 8-bit registers. The results reported in columns (5) and (6), which show the configuration time overhead in clock cycles, demonstrates a significant improvement over the benchmark networks. The number of configuration elements in the generated networks is presented in column (8). Although the proposed methodology aims to reduce the overall access time, the area overhead is also reduced in all cases due to the implementation of the configuration cells with one flip-flop. The experimental results show an average reduction of 87.1% in the overall time overhead compared to the configuration method used in the benchmark networks. This amount changes with the sum of access for every network and improves even further for higher number of accesses. The synthesized networks require an average of 24.7% fewer programmable elements than the original networks.

V. Conclusion

This paper proposed a novel methodology to resynthesize multi-power domain IJTAG networks for improving their timing performance significantly. The newly synthesized network utilizes a remote configuration mechanism yielding an optimized access to the instruments without limiting the instruments' accessibility, as given in the original network. As shown by the experimental evaluation, the presented methodology contributes to the reduction of test costs by enabling 87.1% average reduction in the overall time overhead. In the end, the conducted experiments prove the scalability of the proposed approach even for the large benchmark network representing state-of-the-art design.

TABLE II: Comparing the time and area overhead of the proposed architecture with ITC'16 benchmark networks [25]

(1) **Network**	(2) **Domains**	(3) $\sum$**Accesses**	(4) **CSUs**	**Time Overhead [Clk]**		**Area Overhead [flip-flops]**	
				(5) ITC'16	(6) Proposed	(7) ITC'16	(8) Proposed
Mingle	3	122	50	418	199	26	25
BasicSB	3	88	52	412	130	20	19
TreeFlat	3	515	130	8,880	300	26	19
TrapOrFlap	3	505	188	4,334	462	24	23
q12710	4	1,620	414	7,551	1,137	54	36
a586710	4	1,096	342	8,991	1,173	64	41
t512505	5	9,300	1,211	106,158	22,283	318	238
p22810	6	15,976	1,881	304,958	57,058	540	326
p34392	5	5,095	775	60,679	7,742	194	110
p93791	6	52,245	5,386	2,064,378	256,505	1,192	640
N17D3	4	1,353	264	25,291	897	30	26
N32D6	4	1,055	122	16,657	992	46	31
N73D14	5	6,161	936	276,186	5,881	92	68
N132D4	5	10,174	1,407	828,981	19,749	158	130
NE600P150	6	56,109	5,211	10,261,398	323,766	802	631
NE1200P430	7	189,717	14,275	40,873,068	1,169,386	1,622	1,294

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