Constraint-based Pattern Retargeting for Reducing Localized Power Activity during Testing

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***Abstract*—Highly compact as well as compressed test pattern generation may result in the aggregation of high power activity in specific areas on a manufactured circuit during testing. These hotspots can lead to electromigration and IR-drop in local blocks of the chip resulting in wrong test results. This is due to the circumstance that the effect of localized high switching activity is not precisely taken into consideration during ATPG and pattern simulation. Discarding such patterns may result in test coverage loss. Low power test generation methods typically reduce the switching activity globally across the pattern and not locally in specific areas. Additionally, these methods typically increase the test data volume as well as the testing time. In this paper, a test pattern retargeting methodology is proposed which takes pattern-specific, dynamically identified hotspots into account. Critical patterns and their corresponding critical regions are identified. Based on this data, constraints are used for pattern retargeting preventing the previously identified local hotspots. In contrast to previous methods, the proposed retargeting technique ensures a high test coverage without a large pattern inflation.**

I. Introduction

The power concentrated in specific regions of a manufactured chip may be critical even for low power functional modules. During testing, the problem might be worse since the scan architecture is spanned over the complete chip. The simultaneous test data shifting through the design as well as the test application may result in the congregation of power activity on specific regions on the layout. Typically, test power is much higher than functional power [3], [19]. This aggregated high activity usually results in heat and other effects like electromigration and IR-drop. Sometimes, the concentration of activity during the shift or capture cycle of a test pattern may flip the bit resulting in wrong test results, either masking an error or detecting faults which do not occur in functional mode.

Typically, power analysis tools are used as a sign-off step to check whether the generated tests are power-safe on the layout netlist. These tools perform either rigorous calculations for the determination of power and other effects like IR-drop and electromigration or use approximation techniques with decreased accuracy to save run time. In the industrial tool flow, power-unsafe tests are typically discarded. These discarded patterns result in test coverage loss, which is not desirable. In order to prevent the coverage loss, the remaining undetected faults are usually retargeted by specific low-power Automatic Test Pattern Generation (ATPG) tools. These tools usually relate the power activity to Weighted Switching Activity (WSA) and generate the new patterns with a low global WSA value. However, commercial ATPG tools do not consider any technological information nor the localized WSA on the layout because of the complexity. The low power pattern generation techniques reduce the switching activity globally by keeping its overall value low but does not consider the location of concentrated WSA. Although a global reduction of switching activity has been achieved, localized high WSA may still occur. These high density power areas of low power patterns may still cause pattern failures. The power analysis of low power patterns shows overall power reduction but not the concentrated power density per unit area, which makes certain regions hot as compared to other regions. Additional problems are the determination of the global WSA limit as well as pattern inflation. Generally, low power test generation techniques suffer from the circumstance, that a significant higher pattern count is needed to test the faults resulting in higher test costs. Also, the WSA threshold has to be given as a parameter. If the limit is too strict, the ATPG is not able to generate patterns after reaching the given limit of the global WSA leaving some faults undetected. Thus, there is an urgent need of a feedback loop of the power analysis technique into the ATPG flow. This paper proposes a methodology to incorporate information of the test power analysis in order to regenerate the test patterns in a focused manner. Information about the critical regions are processed and transformed into constraints. These constraints are used during the ATPG retargeting in order to reduce the localized power activity and its effect. Different strategies are discussed in this paper to reduce the aggregation of power activity on the layout. The experimental results show a decrease in power density in the critical areas by, at the same time, high test coverage. Additionally, the number of additionally needed tests is very low. The proposed methodology allows for an easy integration in today's industrial design and test flows.

The organization of the paper is as follows. Section II provides important insights into the related work and state of the art. Section III provides background about the analysis methods used in this paper. In Section IV, the proposed flow and methodology is presented including different strategies. The experimental results are discussed in Section V and conclusions are drawn in Section VI.

II. Related Work

Traditional low power pattern generation methods were introduced at the algorithmic level for the ATPG tools and consider the global test power reduction. Previously, global power reduction techniques were introduced in [6], [26] by simply limiting the number of transitions in the test pattern. The combined approach to reduce both test data volume and scan

power dissipation using test data compression for system-on-a-chip testing was presented in [5]. Another method for power reduction was presented in [24], where a low-capture power X-filling method of assigning 0s and 1s to unspecified (X) bits in a test cube obtained during ATPG is applied. Similarly, other fill techniques like the enable control of clock gates for low power testing in combination with compression were presented in [1]. These techniques reduce the switching activity globally across the pattern during shift and capture phases depending on the algorithm used but without considering the location and other physical phenomenon.

Another compression-architecture-aware ATPG and low power test scheme was presented in [7] in order to reduce toggling rates while feeding test patterns into scan chains. The work in [21] proposes a method for power-aware ATPG, where the test mode power constraints are specified using pseudo hardware logic functions (referred to as power constraint circuits) to minimize test power according to a programmable switching activity threshold, and pattern filtering to isolate patterns which cause high switching activity.

Modified hardware architectures like low power scan cells, power gates, isolation cells and other techniques are also used in industry in order to reduce power consumption. A scan segment skip technique is proposed in [15] to reduce power consumption. A similar kind of low power random test pattern generation scheme is proposed in [25], which disables parts of the scan chains. The method proposed in [16] combines testability-aware test pattern generation with a scan chain disabling technique for low capture power scan testing. A scan cell reordering algorithm to reduce the test power consumption during scan-based testing was presented in [13], whereas a similar scan cell reordering for the test coverage improvement was presented in [8].

A test point insertion approach was presented in [11] for switching activity reduction. In this technique, low-capture-power test points are inserted to reduce the switching activity in critical high-capture-power regions. The proposed approach in [14] reduces scan shift-in switching rates in a user-controlled manner with minimal hardware modifications and elevates compression ratios. These approaches might result in an increase of area thereby increasing the costs.

A proposed design partitioning approach in [23], where any given set of patterns, generated in a power-unaware manner, can be utilized to test the design regions separately. This reduces both launch and capture power in a design-flow compatible manner. Split cycle techniques and multiple power and clock domains are also used in the design to reduce power activity. Sequentially enabling the on-chip clock controllers to generate accurate low power ATPG patterns was presented in [2]. The work in [4] focuses on the management of instantaneous power during the capture phase by taking advantage of the existing clock gating circuitry and selectively holding the value of some scan flip-flops. By this, switching activity during the capture cycles of a test can be reduced. Another similar test pattern generation methodology, which utilizes the available clock-gating mechanism to reduce the launch cycle WSA for at-speed scan testing was given in [17]. However, these kinds of methods affect the timing related features.

Recently, static layout partitioning approaches were also proposed in order to detect and reduce power activity for specific scenarios. An optimization-SAT-based at-speed scan test generation method was proposed in [12]. Here, high-capture-power tests in a pre-generated compact test set are explicitly retargeted. This method employs layout information in reducing capture switching activity in a focused regional manner. The method presented in [18] identifies areas in the layout design, where excessive power consumption likely occurs. However, this is done in a vectorless and probabilistic manner. Another probabilistic and constraint based approach for scan-based low power test generation was presented in [22]. The approach presented in [27] proposed a layout-aware WSA identification flow that evaluates peak current/power on power bumps to detect high power patterns. The above techniques are layout-based but use static partitioning approaches, where the power activity or WSA was obtained via equal partitions on the layout. Besides the fact that the regions have to be fixed before test generation, this may result in boundary errors since the switching activity of the applied tests is dynamical and test pattern dependent. Hence, there is the need for a new approach which is able to identify power critical regions in a dynamic manner as well as to incorporate this knowledge to reduce the power activity in these regions.

III. Light-weight Identification of Power Critical Areas

Since the accurate power and IR-drop analysis is highly resource consuming, especially in terms of run time, only a small subset of test patterns can be accurately analyzed. In previous work [9], [10], we proposed to use a clustering based approximation technique to identify potentially risky regions which uses the Transient Power Activity (TPA) metric instead of the commonly used WSA metric. The TPA metric uses library and cell internal information to achieve more accurate results compared to the WSA metric.

The following steps are used to identify power critical areas:

1) Logic simulation of a test and TPA calculation
2) Application of clustering techniques, i.e. k-means algorithm, in order to relate the TPA values to the layout information
3) Analysis of calculated clusters and identification of power-critical areas on the layout

Typically, test patterns with power-critical areas are discarded since no reliable test result can be guaranteed resulting in test coverage loss. A low-power retargeting procedure to increase the coverage typically suffer from the fact that no information about the power-critical areas is given.

The current work uses these techniques to provide a feedback loop into the test generation procedure in order to incorporate knowledge from the previous analysis. Please note that the procedure is independent from the power analysis technique used as well from the considered metric. These can be easily substituted based on the actual needs.

IV. Proposed Methodology, Flow and Strategies

Test pattern generation is typically done after synthesis and scan insertion and as well as after the physical design step to obtain a test set for the final signoff stage. The test pattern simulation and power analysis are done on the layout netlist before the signoff stage. Hence, any layout modification is usually avoided after this stage. Therefore, we propose to integrate the pattern retargeting as a sub flow or an extended

flow in the test pattern generation and simulation stage of the complete flow.

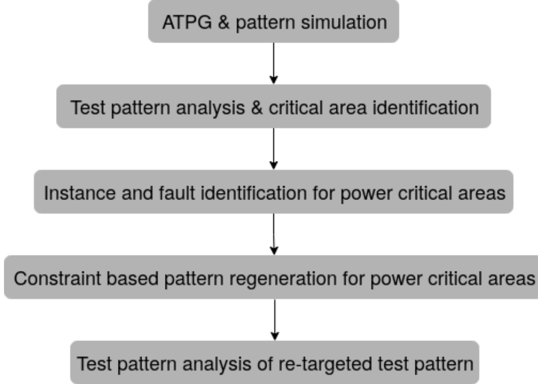

Fig. 1: Proposed flow for pattern retargeting

The proposed flow is shown in Figure 1. The test pattern generation and simulation for the layout netlist is considered as the first stage of the proposed flow. The simulated database provides the information about the switching activity, especially the number of rise and fall transitions of the layout instances. This information along with the layout netlist, technology files, LEF and DEF data is used for the pattern analysis. The second stage, the pattern analysis and critical area identification is done with the help of a clustering technique. Any Local Power Metric (LPM) like WSA or TPA can be used for that purpose. If technology files are available for processing then TPA can be considered as LPM which is more accurate than WSA [9]. Otherwise, the WSA can be calculated based on the fanouts and transitions, as typically used by the ATPG. The k-means clustering technique is used to identify power-critical regions [10]. The patterns corresponding to the critical areas have to be discarded or thrown away since these test patterns may cause IR-drop, local heating effect and other problems resulting into test pattern failure.

After the identification of critical areas, the corresponding instances or gates are extracted followed a the fault identification in the third stage. Given a test set T and a subset $T_p \subset T$, where T_p contains all test patterns which have power-critical regions and should be discarded. Further given a set of faults F_T which includes all faults, which are detected by T and a set of faults F_{T2} which are detected by the test set $T \setminus T_p$. Since the test patterns in T_p are discarded, the faults $F_{\text{undet}} = F_T \setminus F_{T2}$ are not detected anymore resulting in test coverage loss. Consequently, these faults have to be retargeted to guarantee a high test coverage. Therefore, F_{undet} are considered in the following.

We propose to incorporate ATPG constraints into the retargeting procedure. These constraints originate from the pattern analysis. By this, the switching activity can be reduced in a very focused manner without global switching activity reduction resulting in test inflation or coverage loss. Please note that we are only using constraints for the newly generated patterns. In a global view, these constraints are not existent. The test coverage is calculated without these constraints.

Two different strategies are proposed to formulate these constraints. These strategies are explained in detail in the next subsections. The pictorial representation of the critical area identification and the constraints is shown in Figure 2. The newly generated patterns are analyzed again with the pattern analysis to verify the power activity reduction in the last stage.

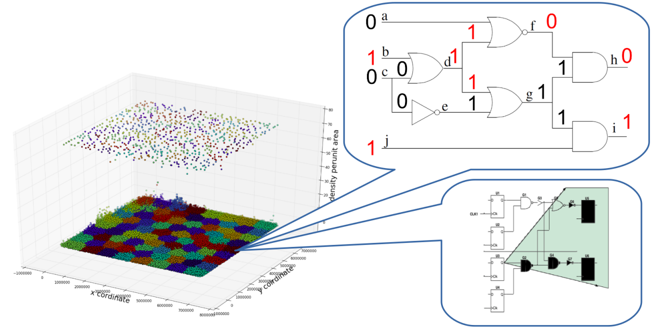

Fig. 2: Instances and faults identification in critical areas

A. Fanout-based method

Given is a critical power activity area R. This area can contain different logical gates including scan elements. The elements of this region are given by $G_r = g_1, \ldots, g_n$. These elements are classified and linked to the corresponding library references in order to find suitable positions for the ATPG constraints.

The main idea to effectively reduce the power activity inside R is to order the elements to the maximum driving load or maximum fanouts.

The elements are subjected to put constraints on the rise transition or the fall transitions depending on the low power factor calculated from the library [9]. The constraints on the pins are set to either 1 or 0 depending on the power rise and fall power factor of the instances. The experiments showed that the fall power factor is mostly used providing a higher benefit in the used libraries.

Because of these constraints, the ATPG will try to find a different suitable pattern for detecting the remaining faults. The newly generated patterns are analyzed again in the next stage of the flow in order to observe the effect of the constraints on the regional activity. In the example, we show ATPG for stuck-at faults for reasons of simplicity. However, the method is also applicable to transition faults. The following example explains the fan-out based strategy for setting ATPG constraints.

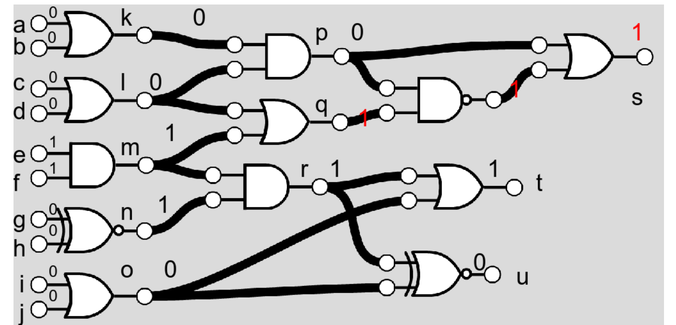

Fig. 3: Stuck-at 0 at point 'q' without constraint

Figure 3 shows the circuit in the critical area R and the original pattern to detect the Stuck-at 0 fault at point 'q'. After analyzing the instances, the maximum fanout strategy is used to set the ATPG constraints on 'p', 'r' and 'o' in order to

reduce rise transitions as well as power activity in R. The newly generated pattern can be seen in Figure 4.

A crucial parameter is the number of ATPG constraints used to reduce the switching activity. A low number of constraints can lead to an ineffective activity reduction, while a high number of constraints can lead to test coverage loss since faults cannot be tested.

Thus, different numbers of ATPG constraints were experimented and the results are discussed in Section V.

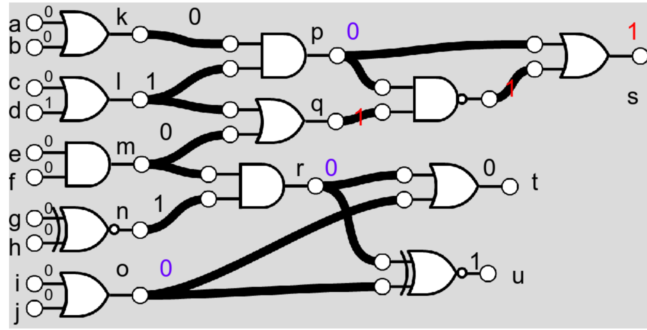

Fig. 4: Stuck-at 0 at point 'q' with maximum fanout constraint

B. I/O trace based method

The effort required to control the ATPG constraints as well as the following effect may also increase or decrease the power activity. Certain ATPG constraints may not be favorable or can cause a decrease in test coverage and hence selecting an appropriate point is critical. As shown in Figure 5, setting a constraint at 'C' may have certain controlling implications in the fan-in cone as well as in the fan-out cone leading to undetected faults and test coverage loss. Hence, in order to access this, another strategy has been developed, where the fan-in and fan-out cones are analyzed as an I/O trace.

In order to reduce the power activity, the instances with the maximum trace were subjected to the constraints. The main idea behind this is that those instances are constrained which have a high influence on the logic. The priority for elements to be constrained depends upon the number of influential elements in the input and output trace.

Again, the elements in the targeted region R are ordered. The structure of the region is analyzed and the size of the fanin and fanout cone of each element is determined (trace). In this ordering, elements with the largest trace come first, since it is important to constrain these to reduce the activity. The higher the influence, the more likely is the instance eligible for constraints in order to reduce power activity.

The following example explains the I/O trace based method.

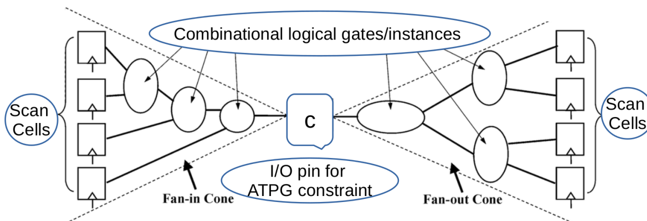

Fig. 5: Fan-in and Fan-out trace

In Figure 6, the Stuck-at 1 fault at 'r' with its corresponding test pattern is shown. In order to reduce the power activity, the maximum traces are determined in the corresponding region. These are further analyzed for selecting the appropriate instances and setting suitable constraints on it according to the library information. The elements corresponding to the trace are constrained to specific values in order to reduce its effect of on the respective fan-in and fan-out cones. The alternative pattern generated for detecting the same fault is shown in Figure 7. The newly generated pattern results in reduced power activity for that region. Again, the number of constraints have an observable effect on the test coverage results and will be discussed in the next section.

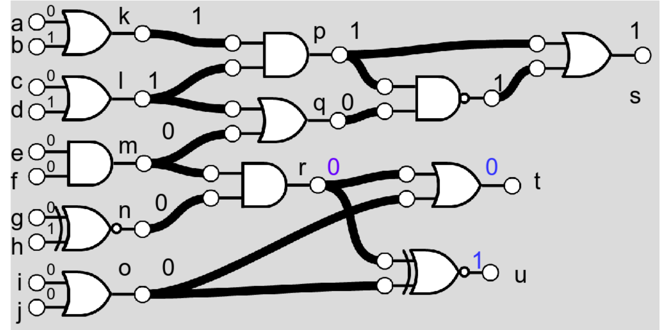

Fig. 6: Stuck-at 1 at point 'r' with without constraint

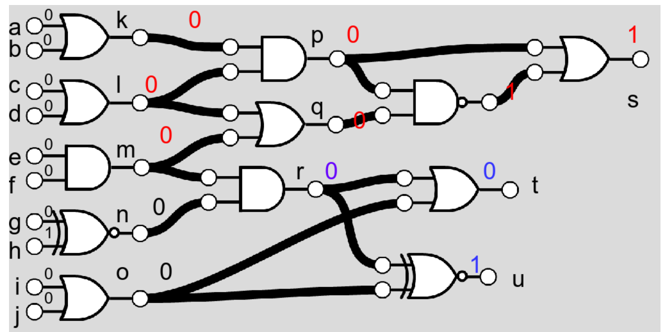

Fig. 7: Stuck-at 1 at point 'r' with maximum trace constraint

V. Experimental Results

The benchmark circuits used for the experiments are OpenCores. The scan synthesis and ATPG is done with the help of commercial tools. The test pattern analysis for identification of power critical areas is done with the help of inhouse tools [10] and python scripts [20]. Other automated post processing scripts are written in Perl. The LPM considered for the experiments is TPA [9] as well as WSA. The capture cycle transitions were considered during stuck-at faults but the method is also applicable to transition faults. Since most of the commercial ATPG tools uses WSA for controlling and rating the power of the patterns during low power ATPG.

The experimental results of the regular pattern generation, low power ATPG and proposed constraint-based ATPG for regional power activity reduction are shown in Table I. The test patterns responsible for power critical areas are discarded after the pattern analysis. The number of discarded test patterns are shown in the 'Original ATPG for critical areas' column. The sub-columns indicate the ATPG parameters i.e. total number

TABLE I: Pattern Retargeting Summary

Benchmarks	Original ATPG for critical areas					ATPG with WSA limitation			Constraint based ATPG					
									Fanout Method			Trace Method		
	Faults	Patterns	#TC	#WCM	#WSM	#WSP	#RP	#TC	#FCM	#P	#TC	#TCM	#P	#TC
ethernet	2519	24	99.90%	18.30%	50.59%	11.00%	42	74.95%	4	52	99.90%	4	41	99.90%
						10.00%	43	73.95%	10	64	99.90%	10	41	99.90%
						9.00%	46	53.28%	20	77	99.90%	20	49	99.90%
						8.00%	60	2.33%	40	92	99.90%	30	59	98.51%
ac97_ctrl	964	22	99.86%	34.64%	51.77%	34.00%	12	71.99%	4	14	99.86%	4	21	99.41%
						33.00%	11	68.46%	10	13	99.85%	10	30	99.22%
						32.00%	14	22.61%	20	17	99.85%	20	34	99.22%
						31.00%	14	15.66%	40	27	99.85%	40	47	97.31%
wb_conmax	8211	31	97.92%	48.39%	51.77%	48.00%	35	97.45%	4	37	97.92%	4	39	97.44%
						47.00%	40	85.76%	10	48	97.92%	10	43	97.02%
						46.00%	52	74.68%	20	58	97.61%	20	52	96.91%
						45.00%	59	12.89%	40	75	97.61%	40	58	96.35%
pci_bridge	1310	24	99.65%	30.74%	51.39%	30.00%	14	92.35%	4	19	99.65%	4	16	97.95%
						29.00%	17	88.42%	10	24	99.65%	10	18	97.91%
						28.00%	18	73.65%	20	28	98.93%	20	22	97.88%
						27.00%	16	22.81%	40	36	98.84%	40	42	97.81%

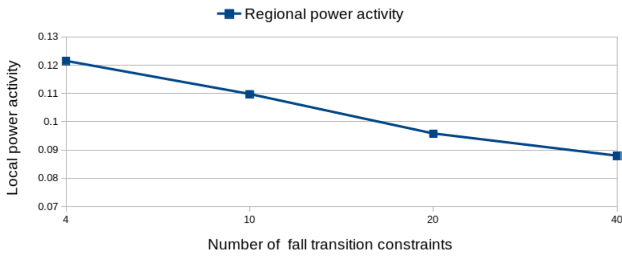

Fig. 8: Local power activity vs. Number of fall transition constraints –wb_conmax

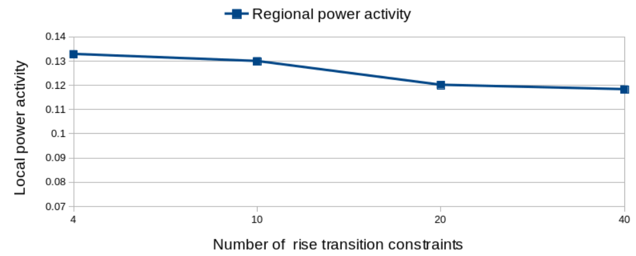

Fig. 9: Local power activity vs. Number of rise transition constraints –wb_conmax

of retargeted faults, the number of retargeted patterns, the overall test coverage(#TC), the maximum capture cycle WSA (#WCM) and the maximum shift cycle WSA (#WSM). For example, 24 power critical patterns detecting 2519 stuck-at faults were discarded for the 'ethernet' circuit.

The traditional low power ATPG methodology generates the low power patterns by limiting the switching activity indicated in the #WSP column. For instance, a value of 10% means that only 10% of the cells are allowed to toggle globally. The number of newly generated low power test patterns is given in column #RP and the overall test coverage is given in the #TC column. It can be observed that decreasing the limit of allowed switching activity leads to an increase in the number of patterns and in a decrease in the test coverage, which is not desirable. The reason is that the limits are too strict for the detection of many faults. Also, this methodology results in a global power activity reduction, but does not guarantee the reduction of power activity in local areas.

In contrast, the proposed constraint-based ATPG reduces the concentrated power activity in the local areas. The number of constraints for the Fanout-based method and the Trace-based method is presented in the #FCM and #TCM column, respectively. The corresponding number of newly generated test patterns and the resulting test coverage are given in the column #P and #TC, respectively. It can be observed that both methods do not cause a test coverage loss as the traditional low power ATPG does. Increasing the number of constraints leads to a test coverage reduction. But the results show that this is very small. Furthermore, it can be observed that the regional power activity can be reduced by increasing the number of constraints. The Fanout-based method generally performs better than the Trace-based methods providing a higher fault coverage.

Figure 8 and Figure 9 depict the comparative decrease in regional power activity for fall transition constraints and rise transition constraints for both methods on the 'wb_conmax' benchmark. It can be seen that the slope of this graph is different, which indicates a difference in power activity for the same number of constraints. It is observed that using constraints for the fall transitions result in lower power activity as compared to the use of constrained rise transitions. Also depending on the strategy used for the constraints, the test coverage is slightly affected but the power activity is considerably reduced with an increase in the number of constraints. Thus the regional power is evenly distributed across the design without much affecting the test costs.

Table II shows the effectiveness of both constraint-based methods in regional power activity reduction for the 'ethernet' design. The pattern number, cluster identifier, cluster's mean X and Y coordinates and the cluster LPM density are given as #PN, #CN, #X_coordinate, #Y_coordinate, #LPM, respectively. It can be observed that the power activity concentrated in the clusters is considerably reduced without much affecting the test coverage as compared to the concentrated power activity in the original ATPG before the pattern retargeting and low power ATPG.

The results show that the overall flow and the incorporation of ATPG constraints originating from the power analysis is able to prevent concentrated power activity in power-critical regions without significantly affecting the test coverage. Fur-

TABLE II: Power critical areas before and after retargeting

Benchmark	Power critical areas before retargeting					Fanout-based method retargeting				
	#PN	#CN	#X_coordinate	#Y_coordinate	#LPM	#PN	#CN	#X_coordinate	#Y_coordinate	#LPM
ethernet	68	8	4698462.81679689	3496302.04384988	0.2316	24	8	4698462.81679689	3496302.04384988	0.1246
	58	8	4698462.81679689	3496302.04384988	0.2297	24	19	4802018.31806843	2067765.44546204	0.1192
	93	19	832755.474521051	5883663.16970539	0.2274	25	18	832755.474521051	5883663.16970539	0.1185
	58	18	4802018.31806843	2067765.44546204	0.2253	31	18	832755.474521051	5883663.16970539	0.1182
						Trace method retarget				
	64	12	4536875.79489819	2545964.79257918	0.2362	37	20	693756.065573923	6195576.65573763	0.1235
	59	12	4536875.79489819	2545964.79257918	0.2284	21	12	4536875.79489819	2545964.79257918	0.1229
	27	20	693756.065573923	6195576.65573763	0.2256	30	12	4536875.79489819	2545964.79257918	0.1220
	64	36	4519962.87895308	3591454.43838604	0.2249	18	20	693756.065573923	6195576.65573763	0.1214

thermore, the method can be easily integrated into today's design and test flows in industrial practice.

VI. Conclusion and Future Work

Traditional low power ATPG does not provide assurance of uniform power activity on the chip during testing. The dynamic creation of concentrated power activity areas on the layout during testing needs to be avoided in order to prevent pattern failures. We have proposed a methodology for pattern retargeting which is able to reduce the switching activity in power-critical regions. A feedback loop is used from the power analysis into the ATPG. Information about power-critical areas are used to formulate ATPG constraints. These constraints are incorporated into the pattern retargeting procedure to produce new tests with reduced activity in the power-critical regions. Two different strategies have been introduced to formulate these constraints. Experiments have shown that this method is able to reduce the activity in the critical regions by, at the same time, high test coverage as well as only a small increase of the pattern count. Furthermore, the strategies allow for a balancing of the number of constraints and the power activity and the test coverage, respectively. Future work involves the reduction in pattern count by a further improvement of the constraint identification.

VII. ACKNOWLEDGMENT

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