Cluster-based Localization of IR-drop in Test Application considering Parasitic Elements

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***Abstract*—Highly compact test patterns are vulnerable to IR-drop during testing which might lead to failures or breakdowns. An accurate analysis of all test patterns is infeasible due to the excessive analysis run time. Previous switching activity based IR-drop prediction methods are highly approximate since less data is used to analyze the test set. In this paper, we propose a dynamic IR-drop prediction methodology, which considers resistive and capacitive parasitic elements of the circuit together with the switching activity. The proposed method uses machine-learning based clustering and is more accurate than the general switching based method. More importantly, the methodology is fast enough that the complete test set can be processed to identify vulnerable patterns prone to IR-drop failure. The experiments show the effectiveness of the proposed approach for the approximate analysis of the complete test set.**

I. Introduction

The testing standards are becoming more complex with the roll out of the sub-nano range process technology. Due to the increasing design sizes (in terms of number of gates), the amount of test data is steadily increasing. The use of DFT and scan architectures leads to a highly non-functional behavior during the test, resulting often in increased switching activity. The high switching of power demand during testing may result into test failures. This failure during testing results into yield loss thereby increasing the production cost per unit. Hence, a pre-production test pattern analysis is typically performed in order to mitigate this effect and identify power-risky tests. This is particularly done for IR-drop [5], [10].

The identification of power-risky tests from the test set is difficult, since previous methods are mainly based on switching activity. However, dynamic IR-drop effects do not only depend on the switching activity but also on the resistive and capacitive elements of the local area. The accurate analysis of all test patterns needs very long run time and can last for weeks or even months for complex designs. Especially the fact that the needed technology-relevant data is only available very late in the design flow makes the analysis infeasible for the complete test set. Previous methods, e.g. using Weighted Switching Activity (WSA), to speed-up the analysis are highly approximate since they are mainly based on toggle information and neglect circuit elements like capacitive and resistive components. ATPG tools typically provide only the WSA values of tests and report only the global power dissipation. However, it is also important to identify localized hot spots. These approximate methods are fast but not accurate enough to provide a reliable result whether a test is power-risky or not.

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In previous work, we proposed a separate test pattern analysis methodology [2], [3], which uses machine-learning techniques to analyze all tests and localize critical areas.

In this work, we improve the proposed methodology for the localization of dynamic IR-drop. Additional parameters are considered to localize the possible voltage drop across the layout more accurately. In the proposed method, we use machine-learning based unsupervised dynamic clustering techniques. Besides technology and layout data as well as the power activity, the integration of parasitic elements like net, pin resistance and capacitance is proposed. A combined view is used to localize possible IR-drop hot spots. This information makes it able to take necessary actions to avoid pattern failure. Even though the method considers limited data, it is able to process all test patterns, which is not possible for highly accurate IR-drop analysis. The experimental results show that the localization can be improved as compared to the previous method.

II. Related Work

The voltage drop across the line or grid area can be ideally estimated with the help of a transistor level model and a simulation, where the current and voltage variation graph and other material characteristics are used to calculate IR-drop. However, applying the same method for a large circuit with billions of transistors is infeasible. For an accurate enough simulation of complex circuits, cell level information is used by EDA tools. However, it still involves a very high computational complexity and much resources [6], [11]. Since it is dependent on various levels of simulation results like SPICE, timing, STA, VCD data etc. it is highly time consuming. Several other methods have been proposed before which are approximate but fast enough to estimate the IR-drop effect. However, most methods deal with the analysis of the functional mode as well as with corner case scenarios and not with test patterns. The method proposed in [8] estimates the IR-drop by using library information and gate level data but in an analytical way. The model used in [7] uses uniform current profiles and some approximations to predict IR-drop at grid centers.

The method proposed in [1] uses Switching Cycle Average Power (SCAP) to correlate and estimate the IR-drop and used it for noise-aware pattern generation for transition delay faults. A similar other method [12] uses global cycle average power as measurement to predict IR-drop for a few at-speed test patterns. However these methods are also approximate and the complete test pattern set cannot be analyzed. In contrast

to previous methods, the proposed method (although being approximate) is able to integrate a large range of data to be more accurate, but still is fast enough to process all test patterns. This makes the methodology suitable to be used for power-risky test pattern identification.

III. Preliminaries

During the system design flow, many analysis and simulation tasks are performed in order to avoid failures and prevent yield loss. The analysis on higher abstraction levels like ESL or SystemC is not much accurate especially for effects like IR-drop since these require the physical implementation. The power analysis, specifically IR-drop analysis, is therefore performed when the physical design is completed and frozen. In the following, the effect of IR-drop is discussed in more detail followed by its consequences on testing.

IR-drop Background: The voltage drop is an unavoidable (even though it may range from mV to nV) phenomenon which occurs in-between the power source and the design unit. The multi-layer structure of the circuit has different metal layers for different routing purposes and other circuits elements layered by deposition, itching and other lithographic processes. The power grid is routed from a supply 'Pin' to power strips at top layers and runs through 'Vias' following different routes to supply 'VDD' at lower layers. Thus, the long route of the 'VDD' to reach each individual circuit element or design unit results into a voltage drop referred to as IR-drop. Due to the material dependent characteristics like resistance, capacitance and other system dependent parameters like switching activity, they are broadly classified into Static and Dynamic IR-drop. Different power grid structures are used like power rings, patches, strips, macro lines etc. at various levels of the die.

ATPG, Test Patterns and IR-drop Failure: The test synthesis involves scan chain formation and the integration of a test architecture during the RTL to GDS synthesis process. Test synthesis is an important step since it also generates the timing related information, scan chain loading-unloading data and other useful information which is used for the pattern generation, simulation, debugging, diagnosis as well as for the Automatic Testing Equipment (ATE) test application in real time. The test patterns are generated with the help of an Automatic Test Pattern Generator (ATPG). This task is performed after the test synthesis.

A generated test pattern may fail during the post-production test due to IR-drop effects and other reasons if precautionary measures are not taken before. Therefore, test pattern simulation, debugging and diagnosis is used to prevent failures during the post-production test. The false capture in scan cells may happen due to timing violations caused by a high voltage drop in that area where a clear cluster of failing flip-flops can be observed. But the tool provides only mesh like information of voltage values or contours of voltage. The remaining diagnosis effort is mostly manual with high human efforts. Whereas in our proposed work, the machine-learning based dynamic clustering helps to identify the scan cells and other instances responsible for the same. With our automated approach, the analysis and planning of further protective actions like pattern retargeting [4] to prevent test failures becomes easier.

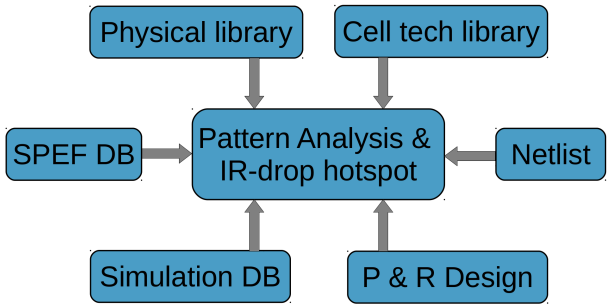

Fig. 1: Proposed analysis with major inputs

IV. Proposed method

The pre-production simulation and power analysis have become sign-off standard. But this kind of power analysis is highly resource consuming. Therefore, it is only performed for the corner cases. However, the corner cases are difficult to predict for testing because most of the test patterns have correlated switching activity. The timing simulation is used to generate switching data, e.g. a VCD file, and huge other databases required to perform dynamic IR-drop analysis. The IR-drop analysis for all the test patterns is not feasible due to excessive run time. Our method addresses this problem by using limited data to approximately identify the test patterns prone to IR-drop failure and localizes the area with clustering techniques. More importantly, it analyzes all the test patterns with more accuracy (compared to WSA) as it considers technology and layout data, as well as parasitic elements.

Figure 1 shows the proposed method and major input blocks. The pattern analysis and IR-drop hotspot block is the processing block which integrates all the data as well as performs the calculations, clustering and smoothed hot spot estimation. The estimation process is explained in the section below. The required data is extracted from different files and used as input. The following itemization lists the information blocks needed for the calculation.

- The cell tech library, i.e. liberty (.lib), is processed to extract the cell features like pin capacitance, resistance and power factors of library elements used for the TPA calculation [2].
- The verilog netlist (.v) is processed to extract the name of instances, nets and other data.
- Physical location features of the cells are extracted from the Layout Exchange Format(.lef) file.
- Physical layout of the design (.def) file is used for the extraction of the location of the power grid, instances, pins, wires, vias etc.
- Parasitic elements values as features are extracted from the SPEF file.
- The test pattern simulation database provides the toggling information of each instance for each pattern. This is particularly used to calculate the TPA values [2].

For the prediction of the IR-drop hotspots for each pattern, we calculate the Transient Power Activity (TPA) value (more accurate version of WSA [2]) for each and every instance in the design. Unsupervised learning-based *k-means* clustering

is then used to dynamically cluster the power activity on the layout [3]. The switching activity (in our case power activity) is a major factor causing the dynamic IR-drop effect. However, it is not the only factor because the resistive and the capacitive features are also important. It may be possible that the power distribution is sufficiently strong enough to drive the load in a high switching area without causing a voltage drop. Vice-versa, IR-drop can be caused when the power or switching activity is low in a particular area but the resistive and capacitive factors are high. Hence, the consideration of capacitive and resistive elements is necessary.

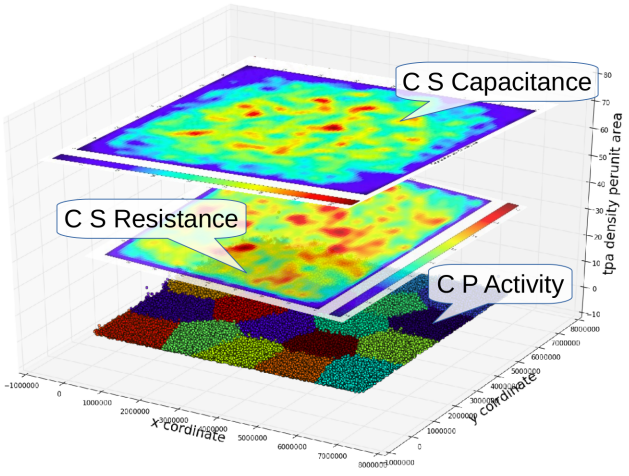

Fig. 2: Clustered smoothing resistance, capacitance and power activity

In the proposed extended approach, the cluster-based method is used to determine the resistive and capacitive profile of the layout. It is followed by a smoothing of the results to estimate and identify the hotspot. Each individual value of a pin capacitance and instance is not useful on its own because of the discrete nature. The dynamically clustered version provides the profile indicating the cluster prone to IR-drop due to the high capacitive nature of the corresponding area as well as the volatility to voltage drop. The latter also depends on the switching in the corresponding area. The clustering of the pin capacitance is performed with the *k-means* clustering approach which is also used to cluster the power activity. Similarly, the net resistance and capacitance values are clustered and the cluster results are stored for the further integration with the switching or power activity clusters.

The complete integration can be imagined as the overlapping of all the cluster results together, i.e. combining the normalized values of the capacitive, resistive and power activity clusters of each test pattern. It is computed with the help of Matrices, where the rows and columns represent the X,Y coordinates and their corresponding values. Figure 2 shows a pictorial representation of the Clustered Power (C P) activity layout layer, overlapped on the Clustered Smoothed (C S) Resistance layer and the Clustered Smoothed (C S) Capacitance layer. The overall output is a new layer which is a combination and overlapping of all these layers according to their X,Y coordinates. This new layer is then smoothed to identify the critical regions. Red-brown areas indicate areas prone for IR-drop which can be further analyzed.

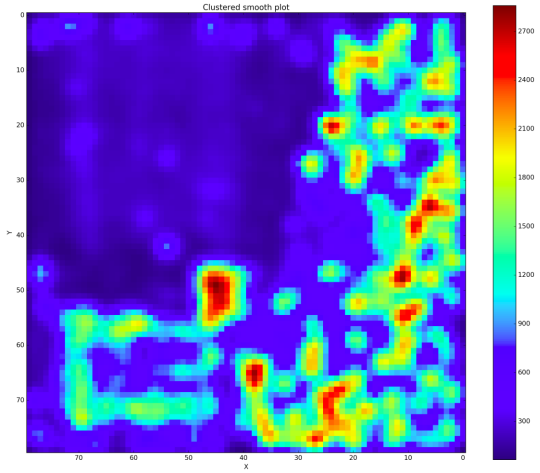

Fig. 3: Estimated IR-drop hotspot of the 'wb_conmax' design

The normalization and smoothing process causes that the values lose their units. Therefore, the result provides the potential dynamic IR-drop areas only and not the actual values of the voltage drop. The advantage of the proposed method is that it does not involve the actual specific voltage drop calculation which is computationally expensive (infeasible for all test patterns) but the combination of the relevant data such as the power/switching activity and parasitic elements in an approximation process to pinpoint to IR-drop prone regions.

V. Experimental Results

The experiments were performed on benchmarks circuits, i.e. OpenCores. Industrial tools were used for synthesis, test pattern generation and simulation purpose. The test pattern analysis, clustering and the complete methodology is performed with the help of inhouse tools [3] and python scripts [9]. For the integration into a design flow, tcl and perl scripting is used. The power metric used for the experiments is TPA [2] as well as WSA.

Table I shows the results of the analysis. The table is divided into two parts. At the left hand side, the results for the analysis without the consideration of parasitic elements is given. At the right hand side, the results of the proposed approach considering parasitic elements are given. Since the dynamic IR-drop estimation is pattern-dependent, the integration of all parasitic elements and the switching activity of each pattern results in different values and hot-spots for each pattern. All the test patterns of a generated test set are analyzed and information about the worst test patterns are shown in the table. The id of the pattern as well as the id for the cluster which were identified as highest IR-drop prone is given. Additionally, X, Y coordinates are given to identify the cluster center and the corresponding Low-power Metric comparative value (#LM). Figure 3 depicts the dynamic IR-drop hot spots estimated for the test pattern number '50' of the 'wb_conmax' benchmark. The normalized local metric does not provide the actual value of the voltage drop but the comparative value with reference to its neighboring values. Additionally, the cluster

TABLE I: IR-drop prone areas without and with parasitic elements consideration

Benchmarks	Before considering parasitic elements					After considering parasitic elements				
	Pattern	Cluster	X_coordinate	Y_coordinate	#LM	Pattern	Cluster	X_coordinate	Y_coordinate	#LM
ac97_ctrl	38	19	978.6563	823.5846	0.1535	6	20	699.4555	811.9013	0.1373
	45	15	577.8820	1178.7561	0.1434	29	28	581.1795	825.2170	0.1328
	27	19	978.6563	823.5846	0.1429	66	30	577.2790	915.9127	0.1308
	26	19	499.2171	799.8614	0.1427	70	28	577.2790	915.9127	0.1299
wb_conmax	30	1	248.4026	931.4846	0.2196	30	3	912.7167	1081.5489	0.1964
	136	36	565.6710	1146.1777	0.2123	118	31	633.6348	1030.2816	0.1958
	93	25	1419.3021	2057.0292	0.2110	161	26	1226.7602	1609.8023	0.1950
	116	17	1026.6603	1190.1135	0.2110	122	3	912.7167	1081.5489	0.1923
pci_bridge32	116	37	1419.0831	428.5870	0.1494	116	31	1264.6494	1080.3577	0.1821
	34	31	1164.9611	617.8995	0.1476	111	14	1126.1164	1446.5122	0.1810
	79	37	1419.0831	428.5870	0.1474	34	14	1126.1164	1446.5122	0.1809
	118	0	1467.6890	1120.4654	0.1426	79	31	1264.6494	1080.3577	0.1775
ethernet	59	12	2268.4379	1272.9824	0.1285	59	12	1983.7354	1253.1622	0.1244
	27	20	346.8780	3097.7883	0.1257	25	9	1286.7491	1633.6190	0.1002
	64	36	2259.9814	1795.7272	0.1250	64	20	1290.4436	2291.5658	0.0997
	59	3	1780.6550	1043.7184	0.1237	14	18	1330.1136	1474.9029	0.0977

data contains the corresponding instance information where the voltage drop is severe.

The identification of the clusters is important since counteractions to reduce the IR-drop depend on the cluster information. When comparing the results of the methods without and with considering parasitic elements, it can be observed that slightly different clusters are identified and the accuracy is increased using the new method. For example, the pattern number '38' and cluster '19' was estimated as critical for the 'ac97_ctrl' design but the capacitive and resistive network was reliable enough. This can be seen by taking the new data into account. The actual worst hotspot was in pattern number '6' and cluster '20' which is the result of the proposed method. The location of this new determined cluster is on the boundary of the old cluster, which can be seen by comparing the Y coordinates. But for some rare cases like 'ethernet', the same cluster (12) and the same pattern number (59) is identified.

In summary, it can be seen that the proposed method which takes more data into account results in a different IR-drop hotspot identification and, by this, increases the accuracy of the IR-drop prediction.

VI. Conclusion and Future Work

Failure analysis of the test patterns is a cumbersome task, the ATPG simulation is insufficient to consider the effects of IR-drop because of the complexity of the calculations. The previous WSA-based methods are technology independent and not much accurate. Whereas the accurate IR-drop analysis of all test patterns is infeasible due to resource constraints. Our proposed methodology balances both accuracy and completeness of the IR-drop prediction for the complete test set. The method is approximate enough, as it considers the power activity and parasitic elements together to estimate the dynamic IR-drop values for each pattern. The method depicts the dynamic IR-drop hotspot along with the clustered result set. The experiments show that the proposed improvement in estimation by considering the parasitic elements are more accurate as compared to previous methods. The cluster-based methodology provides ease of automation by the localization of instances via clusters which helps to take precautionary measures, e.g. regenerating the test patterns to avoid dynamic IR-drop. The approach can be extended in future considering additional design data as well as moving towards simulation-less prediction through machine learning based regression methods.

VII. Acknowledgment

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