Experimental Validation of Memristor-Aided Logic Using 1T1R TaO$_x$ RRAM Crossbar Array

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Abstract—Memristor-aided logic (MAGIC) design style holds a high promise for realizing digital logic-in-memory functionality. The ability to implement a specific gate in a MAGIC design style hinges on the SET-to-RESET threshold ratio. The TaO$_x$ memristive devices exhibit distinct SET-to-RESET ratios, enabling the implementation of OR and NOT operations. As the adoption of the MAGIC design style gains momentum, it becomes crucial to understand the breakdown of energy consumption in the various phases of its operation. This paper presents experimental demonstrations of the OR and NOT gates on a 1T1R crossbar array. Additionally, it provides insights into the energy distribution for performing these operations at different stages. Through our experiments across different gates, we found that the energy consumption is dominated by the initialization in the MAGIC design style. The energy split-up is 14.8%, 85%, and 0.2% for execution, initialization, and read operations respectively.

Index Terms—MAGIC, RRAM, logic-in-memory, fabrication

I. INTRODUCTION

Memristive devices, such as resistive random access memory (RRAM), offer a solution to the von Neumann bottleneck by implementing operations within memory itself [1], [2]. One approach to implementing operations in memory is designing digital logic gates exploiting two distinct states - the high resistive state (HRS) and low resistive state (LRS) of an RRAM. These states are correspondingly mapped to logic “0” and logic “1” respectively. Depending on the input combination stored as a resistive state, the output memristor state can switch from one state to another, representing a logical output value. Several methods for achieving digital logic-in-memory (LiM) have been suggested in the literature. Various stateful and non-stateful logic techniques have been presented in the literature such as IMPLY [3], FELIX [4], majority logic [5], and memristor-aided logic (MAGIC) [6]. Amongst all the techniques, MAGIC stands out as a popular choice because it stores the output in the form of the memristor’s state itself, representing stateful logic.

Experimental validation of MAGIC gates has recently been achieved using fabricated valence change memory (VCM) devices [7], [8]. However, this study specifically focuses on passive crossbar architectures, which suffer from sneak path currents and scalability challenges [9]. The passive crossbars also encounter difficulties during device formation, requiring significant initial current. To address these issues and enhance forming capabilities, a solution involves incorporating a transistor in series with the memristive device. This configuration creates a 1T1R cell, effectively mitigating sneak path problems. The 1T1R cell enables precise current control at the individual device level, offering enhanced control for the MAGIC operations. Despite the increase in physical footprint, the 1T1R configuration renders the overall system more scalable and allows for better control [9].

The MAGIC design style offers the potential for a variety of logic gates. However, the availability of specific logic gates is contingent upon the SET and RESET switching thresholds, which are directly influenced by the material stack used in the fabrication process [10]. The RRAM device based on Pt/TaO$_x$/W/Pt stack offers implementation of OR, NIMP, and 2-cycled XOR gates and has been demonstrated using 1R passive devices [7]. Additionally, in this specific stack configuration, the output device is initialized to the HRS (logic “0”) state, and the input combination, along with execution voltage, determines its transition to the LRS (”1”) from the HRS state.

To the best of our knowledge, for the first time, this paper demonstrates the implementation of MAGIC gates on a 1T1R
energy consumption perspective [11]. Such an analysis is cru-

MAGIC design style in creating general-purpose processing

units, it becomes imperative to examine its design from an

Given the potential application of the

operation phase within the

MAGIC operations.

complete. Additionally, the paper offers a detailed breakdown

to implement any Boolean operation as they are functionally

both OR and NOT gates, which can be effectively combined

The rest of the paper is organized as follows. We provide a

background of the used technique in Section II. Section III

discusses the experimental methods used for logic implemen-

tation and energy estimations. The results obtained from the

study are explained in Section IV. Finally, we conclude the

paper in Section V.

II. BACKGROUND AND RELATED WORK

A. Memristive Devices

Memristive devices have emerged as a significant advance-

ment in non-volatile memory technology. Initially proposed as

a concept by Professor Leon Chua in 1971 [12]. RRAM has

gained prominence due to its unique ability to store data by

modulating resistance states [13]. The resistance modulation

is achieved by applying a voltage across the terminals of the

RRAM. In response, the resistance of the devices changes

based on the magnitude and direction of the current flow.

Remarkably, the memristor preserves its resistance value even

when devoid of power, safeguarding its data until a new

voltage is applied, firmly establishing its status as a non-

volatile memory element [1].

These memristive devices can be interconnected to form a

crossbar structure. However, when individual memristive

devices are connected in a passive crossbar configuration,

issues related to forming and sneak-path currents can arise.

To mitigate these concerns, memristive devices are fabricated

with a CMOS transistor in series, resulting in what is known

as a 1T1R cell. In Fig. 2(a), the SEM image of the fabricated

1T1R cell is shown, with multiple cells interconnected in an

8x4 (rows × columns) crossbar structure (fabrication detailed

is discussed in Section III). Fig. 2(b) provides a schematic

layout of the 1T1R crossbar array. The word lines (WLs) from

1 to 4 are connected to the gates of the devices connected

in columns, while the source lines (SLs) from 1 to 8 are

connected in a row-wise fashion, shorted to all the source pins

of the transistors within the same row. The bit lines (BLs)

from 1 to 4 are connected to the top electrode (TE) pin of

each memristor within a column, as illustrated in Fig. 2(b).

B. MAGIC Design Style

MAGIC represents a stateful logic methodology that em-

ploys crossbar-connected memristive devices to execute logic

operations. Each memristor is programmable to two distinct

states, HRS and LRS, which are subsequently mapped to logic

“0” and “1” respectively. An initialization step is necessitated

to facilitate the MAGIC operations, configuring the output

memristor to its initial state. The range of achievable gates

within these devices is contingent upon the SET-to-RESET

switching threshold ratio. The SET-to-RESET voltage ratio for

the device stack used in our study made logic OR, NIMP, and

NOT gates attainable, diverging from the original NOR and

NOT gates proposed in [6]. The output memristor (yout) is

always initialized to the HRS state rather than the LRS state.

In the OR operation, an execution voltage (Vexe) is applied

to the input memristors (x1 and x2). Simultaneously, the

output memristor, initially set to the HRS state, is grounded,

as depicted in Fig. 2 (c). Furthermore, the NOT operation

necessitates three memristors but with different voltage values

compared to the OR operation. In this context, one of the

inputs is consistently initialized to LRS (designated as x1 for

clarity) in conjunction with the output memristor as shown

in Fig. 2 (d). Additionally, distinct execution voltages (Vexe

and Vexe/3) are employed for the x1 and xin memristors,

respectively.

C. Related Work

The experimental validation of MAGIC design style on

TaOx RRAM devices using passive crossbars has been demon-

strated in existing literature [7]. Nonetheless, passive crossbars

are plagued by the issue of sneak-path currents, which can

disrupt the accurate reading of the final state. Additionally,

forming processes in passive crossbars poses challenges. Non-

stateful logic (e.g., scouting and majority logic) has been

demonstrated using 1T1R cells [14]. This paper represents the

pioneering demonstration of stateful logic on a 1T1R TaOx

RRAM crossbar.
Prior studies have indicated that energy consumption in the MAGIC design style is predominantly influenced by initial-
ization energy [15]. However, it’s essential to note that these findings are primarily derived from simulation studies. Fur-
thermore, the presented energy figures are based on simulation models and pertain specifically to NOT and NOR gates based
on the MAGIC design style. This paper takes strides towards calculating the energy consumption of OR and NOT gates in
fabricated TaOx RRAM devices.

III. EXPERIMENTAL METHODS

A. Device Fabrication

For the experimental validation of MAGIC gates, 1T1R-
Based active memristive arrays were fabricated and integrated
with CMOS 180 nm technology provided by X-FAB. The dimensions of the memristive devices in the arrays are 100 nm x
100 nm and consist of Pt/TaOx/W/Pt stack. Fig. 1 (b) shows
the schematic vertical cross-section of the fabricated device.
Firstly, the W plugs from the processed wafers were exposed,
and the 25 nm thick Pt layer was deposited as the bottom
electrode (BE) with DC sputtering. The BE layer was then
patterned using electron beam lithography and back etching
using reactive ion etching (RIE). A 7 nm thick TaOx layer was
then deposited by RF sputtering in Ar (77%) and O2 (23%)
gas mixture at 236W RF power followed by deposition of 13
nm thick W electrode using the DC sputtering. Subsequently,
a 25 nm thick Pt layer was deposited as TE using the DC
sputtering. Finally, the deposited switching oxide and TE stack
were patterned using electron beam lithography and RIE-based
back etching. Fig. 1(c) shows the SEM image of the fabricated
1T1R TaOx RRAM device.

B. Electrical Characterization Setup

The electrical characterization of the 1T1R memristive
devices was carried out using Keithley 4200 SCS. Fig. 1
(a) shows the schematic of the fabricated 1T1R memristive
device with different terminals. The memristive device in its
pristine state needs a one-time forming step, which involves
the creation of a conductive filament in the switching oxide by
applying a positive voltage across the memristor. The current
through the memristor during the electroforming process is
controlled by applying an appropriate DC gate voltage to avoid
permanent breakdown of the oxide. To realize digital (logic in
memory) LiM using these devices, four distinct operations are
necessary for any logic operation, which are discussed below.

• SET Operation: The SET operation involves changing
  the device’s state from HRS to LRS. This is achieved by
  applying a positive ramp voltage from 0 to 1.8V at the TE
electrode while maintaining a constant DC voltage of 1.6V
on the gate terminal to limit the current flowing through
the memristive to 500μA. The drain and bulk pins of the
transistor are connected to the ground.

• RESET Operation: The RESET operation switches the de-
  vice from LRS to HRS by applying a positive ramp voltage
  from 0 to 2V at the source terminal, while keeping TE and
  bulk grounded. A minimum current requirement is crucial
to dissolve the filament, and if not met, the device remains
in LRS. Achieving this current requirement entails applying
the maximum allowed voltage of 5V at the NMOS gate,
opening the channel for current conduction, and affecting
the minimum transistor size usable with memristors for SET
and RESET processes.

• Execution Operation: During the execution operation, spec-
  ific voltage configurations are applied to memristors for
executing the OR and NOT operations. Once the input
memristors are loaded with the input, the execution voltage
applied across them decides the logic operation being exe-
cuted on them. During this operation, the output memristor
is connected to the ground. The detailed voltage value is
discussed in Section IV-B and IV-C.

• Read Operation: The read operation serves to determine
  the current state of the memristor. A read voltage of 0.5V is
  applied at the TE and the source and the bulk terminals are
  pinned to the ground. A gate voltage of 3.3V is applied at
  the gate to open the NMOS channel during read operation.

Through skillful control of these operations, it becomes
possible to design any arbitrary logic configuration on the
crossbar. In this specific instance, these voltage sequences are
combined to generate OR and NOT gates on the crossbar.
However, these voltage patterns can also be harnessed to exe-
cute complex circuits sequentially or implement architectures
resembling single instruction multiple data. Subsequently, we
look into the outcomes achieved by sequentially applying these
voltages to achieve the desired operations.

IV. RESULTS AND DISCUSSION

Within this section, we unveil the outcomes derived from
our experimental examinations and analyses, offering valuable
insights into the energy consumption associated with the
implementation of MAGIC OR and NOT gates.
A. 1T1R TaOx RRAM Switching Characteristics

The initial forming and subsequent 100 switching cycles are shown in Fig. 3 (a). The memristive devices exhibit counterclockwise switching characteristics. Fig. 3 (b), shows the CDF plot of HRS and LRS states obtained by switching the 1T1R devices 100 times. The device exhibits low cycle-to-cycle (C2C) variation with a consistent HRS/LRS ratio of 10. For evaluating device-to-device (D2D) variability, around 17 devices were switched 100 times each as shown in Fig. 3 (c). From the C2C and D2D variability plots, it is evident that the HRS state exhibits higher variability with resistances distributed over two orders of magnitude ranging from around 100KΩ to 1MΩ. The high variability in HRS can be attributed to the stochastic or uncontrolled breaking of filament during the RESET process [16]. Although the devices exhibit variability in the HRS state, a consistent HRS/LRS ratio of 10 is obtained across all the tested devices and suffices for the implementation of logic gates. Next, we will discuss the execution of logic OR and NOT operations on these devices.

TABLE I

<table>
<thead>
<tr>
<th>TRUTH TABLE FOR OR AND NOT LOGIC GATE OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR</td>
</tr>
<tr>
<td>(x_1)</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

B. MAGIC OR Implementation

Fig. 2 (c) shows the schematic to implement the logic OR gate on the crossbar. To implement OR gate only three memristors are required so this needs to be mapped to the fabricated crossbar with a size of 8x4 as shown in Fig. 2 (c). To map the OR gate on the crossbar, three memristive devices sharing a common WL and a BL in the array are used to implement the gates. Firstly, the inputs of the OR gate are stored as the resistance state in \(x_1\) and \(x_2\). Subsequently, the output memristor (\(y_{\text{out}}\)) is initialized to the “0” state. Next, an execution voltage (\(V_{\text{exe}}\)) sweep from 0 to 3.3V at the TE terminal of \(x_1\) and \(x_2\) and the current at \(y_{\text{out}}\) is monitored. During this cycle, the BL shared by three \(x_1\), \(x_2\) and \(y_{\text{out}}\) is kept floating. While WL/\(V_{\text{G}}\) is connected to a DC voltage of 3.3V and the SL of the output memristor is grounded. All the other unused WLS, SLS, and BLs are kept floating. Post-execution cycle, the state of \(y_{\text{out}}\) is obtained by performing a READ operation. The memristor output currents during execution cycles for different inputs are shown in Fig. 4.

The truth table for the OR gate with the input and output states of the memristor are shown in Table I. In Table I, \(y_{\text{init}}\) column shows the initialization state of the output memristor before the execution cycle. It can be inferred from the truth table that for successful OR gate operation, the \(y_{\text{out}}\) changes its state for all combinations of inputs except for the input “00” during the execution cycle. Fig. 4 shows the execution cycles for different input combinations. For the input “00” case, both \(x_1\) and \(x_2\) are in HRS state represented by the current value \(I_{\text{in1}}\) and \(I_{\text{in2}}\), respectively. When an execution voltage is applied at the inputs, the current through the \(y_{\text{out}}\) is limited by the parallel combination of \(x_1\) and \(x_2\). This current is not sufficient to drive the \(y_{\text{out}}\) to the SET state. This is evident from the fact that no sharp change in output current (\(I_{\text{out}}\)) w.r.t applied \(V_{\text{exe}}\) is observed in the \(y_{\text{out}}\) as shown in Fig. 4 (a).
On the other hand, for the input combination of “01”, “10”, and “11”, either one or both of the input memristors are in LRS states. This allows a sharp increase in $I_{out}$ during the execution cycle, contributing to the change of state of $I_{LRS}$ states. This allows a sharp increase in current. Fig. 7 summarizes the output read currents for different input read current combinations and successfully demonstrates NOT gate.

**D. Energy Calculations**

The energy consumption of logic operations is heavily dependent on the initialization as well as execution energies. In earlier works, researchers have typically calculated the energy consumption of a log-in memory system through a coarse-grained approach by multiplying the average energy of operations by the number of operations [17]. However, this method has been found to underestimate the actual energy consumption as it ignores the initialization energy involved during the operations [15], [18]. However, these results are in the simulation and with different memristor models. Therefore, in the current study, a similar approach has been considered for real devices, for calculating the energy consumption of logic operations by taking execution as well as initialization energy into account.

During OR operation, the different initialization steps involve numerous SET and RESET operations as mentioned in Table III. In the study, triangular wave sweep voltages are used to perform, SET, RESET, and READ as well as execution operations. The energy is obtained by multiplying the voltage waveforms with the sensed current and then integrating the product over the measurement time as per $\int_0^t v(t) \times i(t) \ dt$, where $t$ is the pulse time considered for energy calculations. The I-V curves corresponding to median SET and RESET operations are shown in Fig. 8. Two approaches have been used for calculating the energy: a) using full voltage ramp cycle time and b) using optimum times. In the first technique, energy is calculated for the whole triangular voltage sweep. In contrast, in the case of optimum energy calculation, the SET, RESET, and execution times have been derived from the experimental data, and energy is calculated for the same as shown in Fig. 8.

The former technique gives actual energy consumption numbers but is an overestimate. Therefore, for more realistic energy values, the latter technique is used. Table IV summarises the energy consumption for OR and NOT gate operation through both techniques. It is quite evident that for both the optimal and full voltage ramp cycle-based energy calculations, depending on the inputs of the OR operation, around 35-85% of the energy consumption is constituted by the initialization energy, execution energy constitutes around 64.8-14.8% while read energy only constitutes around 0.2% of energy. Evidently, as the accuracy of energy calculation

**TABLE II**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Voltage(sweep)</th>
<th>Pulse duration ($\mu$s)</th>
<th>Energy(nJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET</td>
<td>0 to 2 V</td>
<td>4 ms</td>
<td>1300</td>
</tr>
<tr>
<td>RESET</td>
<td>0 to 1.8 V</td>
<td>3.6 ms</td>
<td>312</td>
</tr>
<tr>
<td>LRS Read</td>
<td>0 to 0.3 V</td>
<td>0.6$\mu$s</td>
<td>5.4</td>
</tr>
<tr>
<td>HRS Read</td>
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<td>0.6$\mu$s</td>
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increases, the gap between total energy and execution energy also increases. Therefore, for accurate calculation of energy consumption for logic operations using the MAGIC technique, the initialization energy must be taken into consideration.

### V. CONCLUSION

In this paper, TaO$_x$ RRAM devices were fabricated and integrated on a 180 nm CMOS substrate to create a 1T1R crossbar array. The fabricated devices consistently exhibited an HRS/LRS ratio of approximately 10, making them eligible for the implementation of MAGIC gates. Subsequently, we demonstrated the implementation of logic OR and NOT gates, and along with energy consumption values. Energy consumptions for logic OR and NOT operations were calculated by evaluating both the initialization and execution energies. It was found that the initialization energy played a significant contributing role in the overall energy consumption during logic implementation, similar to the trends observed in the simulation study.

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