An ILP-based Global Optimum Test Scheduler for IEEE 1687 Multi-Power Domain Networks

Payam Habiby[†]

Sebastian Huhn*†

Rolf Drechsler*†

*University of Bremen, Germany {habiby,huhn,drechsler}@uni-bremen.de

[†]Cyber-Physical Systems, DFKI GmbH 28359 Bremen, Germany

Abstract—The IEEE 1687 standard defines a methodology for accessing embedded instruments in the state-of-the-art system-on-chips by introducing reconfigurable scan networks. This methodology enables a considerable reduction of the overall test time by shortening the length of the active scan chain. However, this new technique raises the need for effective test schedulers considering individual instruments' constraints and multiple power domains. By this, it is ensured that the power criteria are met during the later test execution. This work tackles the arising challenges by proposing an entire test scheduler for multi-power domain LJTAG networks based on an integer linear programming optimization model. In contrast to existing works, the proposed scheduler determines the global optimal test sequence and, by this, yields the most effective and powersafe tests.

I. INTRODUCTION

The IEEE 1687 Std. [1] (IJTAG) has been introduced to tackle the challenge of long scan chains in modern System-ona-Chip (SoC) by providing flexible access to the instruments through reconfigurable scan networks. In Fig. 1(a), an exemplary IJTAG network is shown containing four instruments Inst. 1 to Inst. 4 that are divided into two power domains, as indicated by different colors. These instruments can be accessed individually or concurrently depending on the configuration of Segment Insertion Bits (SIBs) and ScanMux Control Bits (SCBs). These programmable elements receive their 1-bit configuration data serially along with the test data in every Capture-Shift-Update (CSU) cycle. Typically, the instruments in the network require a different number of accesses. An instrument or sub-network with completed access can be excluded from the network by resetting the corresponding SIB to 0, as is shown in Fig. 1(b). By this, the IJTAG network enables to shorten the length of the scan chain and, hence, allows to reduce the number of required configuration bits that must be appended to the test data for every test session. However, minimizing the test time still depends on the sequence over which the instruments are accessed, strictly requiring the use of effective test schedulers. The flexibility of IJTAG networks, along with the implementation of multiple power domains in modern SoCs, poses new challenges for test scheduling, for instance, due to non-linear constraints.

Significant research has been carried out to reduce the overall test time while taking benefit from reconfigurable scan network structures [2]–[10]. In [11], a graph-based model of

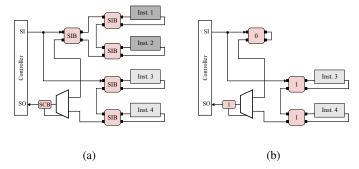


Fig. 1: An example of an IJTAG network

IJTAG networks has been proposed to detect the concurrently accessible instruments in multi-power domain networks. A *Boolean Satisfiability* (SAT)-based model for test retargeting in reconfiguration networks is introduced in [12]. This SAT-based model has further been extended by work [13] to improve the test scheduling time using incremental pseudo-Boolean optimization techniques. Although the achieved results of these previous works are already quite promising; they still do not guarantee a global test time optimization.

This work proposes a novel test scheduler for IJTAG networks with multiple power domains using *Integer Linear programming* (ILP) techniques, which has also been used to solve many practical problems [14]. The proposed ILP-model is processed by well-engineered formal solving engines yielding global optimal power-safe tests and, hence, allowing for a significant test cost reduction.

II. PROPOSED ILP OPTIMIZATION MODEL

This section describes the proposed optimization model implementing the test scheduler for IJTAG networks. More precisely, the proposed model minimizes the number of required CSUs used for the instruments' test and, hence, determines the minimum overall access time without exceeding the power domains' limits. In particular, ILP is being orchestrated, yielding a mathematical optimization problem with integer variables, in which the objective function and constraints are linear. The basic principle can be defined as follows:

minimize / maximize
$$c^T x$$
 (1) subject to $Ax < b, x \in \mathbb{W}$

where x represents the vector of decision variables with real coefficients c, and $A = [a_{ij}]_{m \times n}$ is a matrix with $a_{ij} \in \mathbb{R}$, creating the constraints bounded to $b \in \mathbb{R}$.

A. Objective Function

The overall instrument access time can be reduced by concurrently accessing as many instruments as possible. In fact, the optimal distribution of the CSUs over the concurrently accessed elements forms an important aspect for minimizing the overall instruments' access time. In the worst case, every instrument has to be accessed individually through an exclusive scan chain. This implies that in an IJTAG network with n instruments, the upper bound for the number of required scan chains equals n. In such a network, the resulting $n \times n$ decision matrix $M \in \mathbb{B}^{n \times n}$ is defined as follows:

$$M = \begin{bmatrix} x_{11} & x_{12} & \dots & \text{inst. } n \\ x_{11} & x_{12} & \dots & x_{1n} \\ \vdots & & & & \vdots \\ x_{n1} & x_{n2} & \dots & x_{nn} \end{bmatrix}$$
 chain n

The Boolean variable x_{ij} decides on the inclusion or exclusion of j-th instrument of the i-th chain. The number of accesses, power consumption, and power domain of this instrument are given as a_i , p_j , and d_j .

Each row of M represents a scan chain used for the test data transfer to the instruments if the corresponding Boolean variable is set to 1. Consequently, every column of M shows the engagement of an instrument over different scan configurations during the test. If all of its decision variables are set to 0, the corresponding chain is excluded from the final scheduling. All the active instruments, that are represented in a row of M, perform the same number of CSUs and, hence, are accessed equally. By assuming a_i as the number of CSUs in row i of M, the optimization's aim is about minimizing the sum of these values in the final decision matrix. Thus, the objective function is defined as follows:

$$Min\sum_{j=1}^{n} a_i \tag{2}$$

By construction, it is guaranteed that the ILP solver minimizes the number of totally required CSUs to cover all the instruments of the IJTAG network and, consequently, optimizes the overall test time.

B. ILP Constraints

A valid solution of the objective function defined by Equation (2) must fulfill three types of constraints. The first one concerns the overall power limit of each power domain, the second one addresses the number of required accesses for each instrument, and the last one considers the structural connectivity of the network components, as described in the remainder of this section.

Power constraints: Let p_{ij} be the power consumption of the j-th instrument of the i-th row of the decision matrix M,

which is located in power domain k, and $P_{max,k}$ be the power limit of the k-th power domain. Since the accumulated power consumption of active instruments in each power domain should not exceed the domain's power limit, the following constraint must hold for every row of M:

$$\sum_{x_j \in k} x_{ij} \cdot p_j \le P_{max,k} \qquad 1 \le k \le K \qquad 1 \le i \le n \quad (3)$$

For an IJTAG network with n instruments and K power domains, this creates a total of $n \times K$ power constraints. **Access constraints** guarantee that every instrument can obtain its total A_j required number of accesses over the different scan chain configurations.

$$\sum_{i=1}^{n} x_{ij} \cdot a_i = A_j \qquad 1 \le j \le n \qquad a_i, A_j \in \mathbb{W} \qquad (4)$$

This non-linear constraint is transformed to a linear constraint by introducing the new decision variable $y_{ij} = x_{ij} \cdot a_i$ and then using Glover's linearization [15]:

$$\sum_{i=1}^{n} y_{ij} = A_{j} \qquad 1 \le j \le n \qquad y_{i}, A_{j} \in \mathbb{W}$$

$$0 \le y_{ij} \le Ax_{ij} \qquad , \qquad a_{i} - A(1 - x_{ij}) \le y_{ij} \le a_{i}$$

$$(5)$$

where A is the maximum number of given instrument accesses. Considering these assumptions, the new decision matrix \bar{M} is defined as follows:

$$\bar{M} = \begin{bmatrix} y_{11} & \dots & y_{1n} \\ \vdots & \ddots & \\ y_{n1} & \dots & y_{nn} \end{bmatrix}.$$

If the j-th instrument in i-th session is activated, the corresponding element in matrix \bar{M} would be a_i and, otherwise, is assigned to 0 representing that no access is scheduled for the instrument in ith session. The inequalities in Equation (5) guarantee that y_{ij} evaluates to either 0 or a_i .

Structural constraints investigate the feasibility of concurrent placement of different instruments on a chain. Modeling the IJTAG network in a CNF format has been described in [13]. Each clause of this CNF can be transformed to an ILP constraint and added to the overall instance. As an example, two successive network elements x_1 and x_2 with the given CNF are transformed as follows:

$$\Phi = (x_1 \lor \neg x_2) \land (\neg x_1 \lor x_2) \implies x_1 - x_2 \ge 0$$
$$-x_1 + x_2 \ge 0$$

The proposed objective function over Boolean variables in combination with the presented integer linear constraints yields a seamless ILP model representing the IJTAG instruments' access problem that is to be solved by powerful ILP solvers.

TABLE I: Test scheduling in Mingle network for different access scenarios

scenario	#accesses								#CSUs	
	$\overline{w1}$	w2	w3	w4	w5	w6	w7	$\overline{w8}$	PBO [13]	ILP
1	32	18	20	12	10	25	35	13	90	85
2	28	36	42	19	22	17	10	50	123	121
3	23	60	98	39	52	73	18	42	245	208
4	130	215	170	163	211	83	315	97	786	745
5	250	515	370	463	441	603	375	282	1931	1809
6	342	294	460	611	370	394	436	229	1736	173

III. EXPERIMENTAL RESULTS

The experimental evaluation of the proposed test scheduling method is presented in this section. The framework implementing the scheduler is written in C++, and the results are obtained using a machine holding an Intel Xeon E3-1270 processor and 32GB of main memory. Different instrument access scenarios are designed for Mingle network from the ITC'2016 benchmark suite. The results are given in Table I, which compares the number of required CSUs of the proposed method and PBO of [13].

The eight instruments w1-w8 of the Mingle network with power consumption $\{85, 93, 110, 115, 76, 134, 125, 100\}$ are divided into two power domains holding the instruments $\{w1,w2,w5,w6\}$ and $\{w3,w4,w7,w8\}$ with domains' power limits 140, respectively. The scenarios with randomly generated accesses in Table I show improvement of the overall test time in CSUs over the previous method. Table II reports the results of PBO and ILP test scheduling for different IJTAG benchmark networks.

For the experiments, a non-successive scheduling is considered, i.e., the scheduler is not required to access an instrument in successive sessions. This scheduling principle provides more flexible schedules resulting in shorter test time. The scale and complexity of the networks are given as the number of nodes and edges obtained from the networks' graph model introduced in [11]. In all experiments, the elements are divided into three power domains with given power limits. The power consumption values are randomly created and the sum of power consumption in each domain is presented in column \(\sum \) power. The rightmost columns show the number of required CSUs and scan chains that can cover a total of \sum acc. instrument accesses in both PBO and ILP methods. The access time obtained by ILP scheduler, which is presented in terms of CSUs, is either improved in comparison to PBO method or confirms its optimality.

IV. CONCLUSION

This paper proposed a novel ILP-based test scheduler optimization scheme for multi-power domain IJTAG networks. More precisely, a framework has been implemented in C++ that supports the IJTAG's inter-connectivity language and uses the CPLEX ILP solver [16] yielding a global optimal and power-safe test schedule and, hence, can be employed to evaluate the performance of other test schedulers.

V. ACKNOWLEDGMENT

This work was supported by the AI initiative of the Free Hanseatic City of Bremen.

TABLE II: Results of non-successive test scheduling for ITC'16 benchmark networks using PBO and ILP methods

network	(nodes, edges)	power domain			∑acc.	#CSU		#chains	
		ID	∑power	limit		PBO	ILP	PBO	ILP
Mingle	(27, 39)	1	27	20	200	114	114	8	8
		2	410	140					
		3	428	140					
BasicSCB	(33, 42)	1	34	30	88	52	52	5	5
		2	328	180					
		3	473	180					
TreeFlat	(38, 61)	1	13	30	158	30	26	8	10
		2	530	330					
		3	412	290					
q12710	(52, 78)	1	52	55	377	191	191	21	22
		2	1177	160					
		3	1274	170					
t512505	(289, 447)	1	130	30	1684	476	427	110	92
		2	4458	190					
		3	5040	180					
N17D3	(52, 66)	1	53	55	488	174	173	27	24
		2	1378	200					
		3	1066	150					
N32D6	(79, 101)	1	79	100	655	119	117	35	37
		2	1478	200					
		3	1812	250					
N73D14	(155, 200)	1	94	100	900	120	120	12	12
		2	3444	300					
		3	3468	300					

REFERENCES

- "IEEE standard for access and control of instrumentation embedded within a semiconductor device," IEEE Std. 1687-2014, pp. 1–283, 2014.
- [2] S. S. Nuthakki, R. Karmakar, S. Chattopadhyay, and K. Chakrabarty, "Optimization of the IEEE 1687 access network for hybrid access schedules," in *IEEE VLSI Test Symposium*, 2016, pp. 1–6.
- [3] S. Gupta, A. Crouch, J. Dworak, and D. Engels, "Increasing ijtag bandwidth and managing security through parallel locking-sibs," in *IEEE International Test* Conference, 2017, pp. 1–10.
- [4] S. Gupta, J. Wu, and J. Dworak, "Efficient parallel testing: A configurable and scalable broadcast network design using IJTAG," in *IEEE VLSI Test Symposium*, 2018, pp. 1–6.
- [5] R. Baranowski, M. A. Kochte, and H. Wunderlich, "Scan pattern retargeting and merging with reduced access time," in *IEEE European Test Symposium*, 2013, pp. 1–7.
- [6] S. Keshavarz, A. Nekooei, and Z. Navabi, "Preemptive multi-bit IJTAG testing with reconfigurable infrastructure," in *IEEE International Symposium on Defect* and Fault Tolerance in VLSI and Nanotechnology Systems, 2014, pp. 293–298.
- [7] M. A. Kochte, R. Baranowski, and H. Wunderlich, "Trustworthy reconfigurable access to on-chip infrastructure," in *IEEE International Test Conference in Asia*, 2017, pp. 119–124.
- [8] R. Krenz-Baath, F. G. Zadegan, and E. Larsson, "Access time minimization in IEEE 1687 networks," in *IEEE International Test Conference*, 2015, pp. 1–10.
- [9] F. G. Zadegan, U. Ingelsson, G. Asani, G. Carlsson, and E. Larsson, "Test scheduling in an IEEE p1687 environment with resource and power constraints," in *IEEE Asian Test Symposium*, 2011, pp. 525–531.
- [10] R. Cantoro, M. Palena, P. Pasini, and M. S. Reorda, "Test time minimization in reconfigurable scan networks," in *IEEE Asian Test Symposium*, 2016, pp. 119–124.
- [11] P. Habiby, S. Huhn, and R. Drechsler, "Power-aware test scheduling for IEEE 1687 networks with multiple power domains," in *IEEE International Symposium* on *Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, 2020, pp. 1–6.
- [12] R. Baranowski, M. A. Kochte, and H.-J. Wunderlich, "Reconfigurable scan networks: Modeling, verification, and optimal pattern generation," ACM Transactions on Design Automation of Electronic Systems, vol. 20, no. 2, 2015.
- [13] P. Habiby, S. Huhn, and R. Drechsler, "Optimization-based test scheduling for IEEE 1687 multi-power domain networks using Boolean satisfiability," in *International Conference on Design Technology of Integrated Systems in Nanoscale Era*, 2021, pp. 1–4.
- [14] D.-S. Chen, R. G. Batson, and Y. Dang, Applied integer programming: modeling and solution. John Wiley & Sons, 2011.
- [15] F. Glover, "Improved linear integer programming formulations of nonlinear integer programs," *Management Science*, vol. 22, no. 4, pp. 455–460, 1975.
- [16] IBM, ILOG CPLEX Optimization Studio, 2021. [Online]. Available: https://www.ibm.com/docs/en/icos/20.1.0?topic=cplex