System Level Verification of Analog/Mixed-Signal Systems using Metamorphic Relations

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***Abstract*—*Metamorphic Testing* (MT) has been employed very successfully in the software domain. The core idea is to uncover bugs by relating consecutive executions of the program under test. In this paper, we present a novel MT-based verification approach to verify *Analog/Mixed-Signal* (AMS) systems at system level. The central element of our MT-approach is a set of *Metamorphic Relations* (MRs) which describes the relation of inputs and outputs of consecutive DUV executions. We demonstrate the effectiveness of our MT-based verification approach on *Low Noise Amplifiers* (LNA) and *Phase-locked Loop* (PLL).**

I. Introduction

The interaction of analog/*Radio Frequency* (RF) structures and digital logic has increased significantly in modern *Analog/Mixed-Signal* (AMS) systems. As a consequence methodologies are required to design, verify and produce high quality AMS systems cost-effectively. However, several challenges are faced: (1) Quick and fast modeling to make the right design decisions, (2) fast simulation of application scenarios, and (3) novel cost-effective verification methods. Some of these issues are addressed by system level solutions which have made there way into industry. In particular, SystemC AMS-based modeling and verification is heavily used today [1], [2], [3], [4]. However, one of the main challenges is the availability of reference models for verification. Since formalizing the RF/AMS behavior is non-trivial and very time-consuming, manual (and most often visual) analysis of the waveforms is carried out in industrial practice.

To overcome this problem, recently a new verification perspective has been introduced in the software domain: *Metamorphic Testing* (MT) [5] which alleviates this problem. Instead of relying on the reference value computed from reference models, MT looks at *Metamorphic Relations* (MRs), i.e. how the inputs and outputs of multiple *Design Under Verification* (DUV) executions relate. Let us consider an example: Assume the goal is to test a program implementing the *sine* function *prg_sin(x)*. Based on the well known trigonometric properties we can use *sin(x) = sin(x + 360)* as MR. Instead of checking the expected output for a concrete input to the program, we can run the program for an input x_1 and afterwards for the input $x_2 = x_1 + 360$ (follow up test-case). Now, using the above MR we just have to check if *prg_sin*(x_1) = *prg_sin*(x_2). If this is not the case, we have found a bug.

Contribution: In this paper we propose a MT-based verification approach to effectively verify the AMS systems at system level. We consider two industrial AMS systems – *Low Noise Amplifier* (LNA) and *Phase-Locked Loop* (PLL). We devise a set of 12 and 8 generic MRs, respectively [6], [7]. As reference models are not required to ensure correctness when performing MT, the investment to use the proposed MT-approach is low. However, the potential benefit in design verification is huge. In an extensive set of experiments on industrial configurable system-level models, our proposed MT-approach found serious bugs which escaped during the regular verification process.

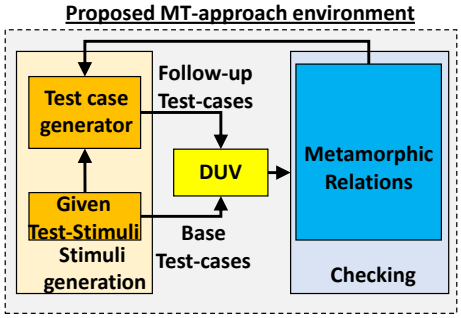

Fig. 1. High-level block diagram of the proposed MT-based verification approach

II. MT-based System Level Verification Approach

A high-level block diagram of the proposed MT-based verification approach is shown in Fig. 1. It consists of three major components: *Stimuli generation*, *Metamorphic Relations* (MRs) and *Checking*. MR is a necessary property of the target function (so in our case LNA and PLL) in relation to multiple inputs and their expected outputs. *Stimuli Generation* uses the given test-stimuli, i.e., test-stimuli used during the regular verification process, and MRs to generate follow-up test-cases. The given test-stimuli and the follow-up test-stimuli are input to the DUV to exercise different behaviors of the model. The *Checking* block in combination with MRs collects DUV outputs for performing relation checks, i.e., comparison of LHS and RHS according to the MRs. To leverage MT for verification of AMS systems, the central element of MT, i.e., set of MRs, has to be identified. Linearity of an LNA is one such property where the LNA increases the power level of an input signal without altering the content of the signal. The MR could be: The output voltage of LNA scales by the same factor with which the input voltage is scaled. Let x_1 be the base test-case and N is the scaling factor, and the amplifier is in linear region, then the following should always hold

$$N \times LNA_{output\_voltage}(x_1) = LNA_{output\_voltage}(N \times x_1)$$

Similarly, one MR for PLL could be: The *Charge Pump* (CP) generates pulses of positive or negative currents based on its digital inputs. The following relation should always be

satisfied over 2 executions of the CP:

$$Current[CP(IN_1, IN_2)] = -Current[CP(IN_2, IN_1)]$$

As shown, MRs require multiple executions of the DUV with varying inputs. Hence, multiple test-stimuli are required which build on top of a base test-stimuli. The test-stimuli from the verification plan created during the regular verification process are a good candidate as a base test-stimuli. Therefore, we use them as base test-stimuli. Verification of the correct DUV behavior is carried out in the *Checking* block. As motivated earlier, MRs don't need reference models. Hence, the *Checking* block performs relation checks, i.e. compares the LHS and the RHS of MRs. If both the sides of the MR are equal, the MR passes, otherwise it fails.

The investment to use the MT-based verification approach is low. However, the potential benefit in design verification is huge. In the next section we present an extensive set of the experiments on industrial system-level models using the MT-based approach.

III. Experiments

In this section we present the experiments to demonstrate the effectiveness of our approach for the verification of AMS systems. For the experiments we use a configurable system-level model of an LNA and PLL provided by our industrial partner. The models have been implemented in SystemC-AMS. The models come with a set of test-stimuli created according to the verification plan, i.e. an intensive verification of different behaviors of the models has already been performed by our industrial partner. Hence, they do not expect any faults in the model. However, we have found serious bugs in the LNA and PLL using the presented MRs [6], [7], which escaped during the extensive verification performed by our industrial partner.

A. Case Study: Low Noise Amplifier

In this case study, we use the test-stimuli which have been shipped together with the model as mentioned in the previous section. As expected the LNA specifications have been verified with the given test-stimuli and no faulty behavior was observed. At this point we employed our MT-approach using the given test-stimuli as the base test-cases. The follow-up test-cases were created with our MT-approach based on the MRs from [6]. Hence, without any manual effort our MT-approach immediately found the violation of two MRs. The output power and the corresponding gain did not follow the *core properties* of the LNA. Upon close manual inspection of the waveform (Fig. 2, we observed a slight overshoot of the gain curve for a short duration before settling to a stable value in the saturation region. Erroneously, the analog designer has chosen to use *Taylor Series Expansion* in the approximation algorithm of LNA model for the non-linear behaviors and did not consider the occurrence of higher-order polynomials [8]. This bug was discussed with our industrial cooperation partner and they decided to fix the model accordingly using the concepts from [9]. Afterwards, no further bugs were found with our MT-based verification approach.

B. Case Study: Phase-Locked Loop

As expected, the simulations for the set of shipped test-stimuli passes. As a next step, we employed our proposed MT-approach using the given test-stimuli as the base test-cases.

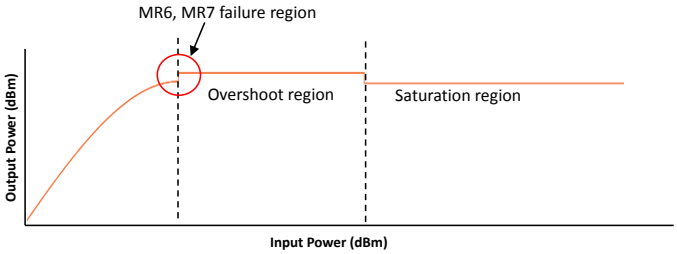

Fig. 2. *LNA* Output power vs Input power (dBm) and MR6, MR7 failing [6]. Overshoot of output power because of non-linearity approximation.

The MRs from [7] were used to create the follow-up test-cases. Running our MT-approach with the proposed MRs resulted in a failure. Close inspection of the waveforms revealed that the PLL was locking to a different very low frequency. This is called the **Dead-zone** effect. A **Dead-zone** occurs when the PLL loop does not respond to small phase errors. Looking into the design of *Phase Frequency Detector* (PFD) revealed that there was no delay element between the *AND* gate and the *reset* pins of the Flip-flops. The delay element between the output of *AND* gate and the *reset* inputs of Flip-flops ensures that dead-zone effect does not happen. After insertion of the delay element, we observed the correct output behavior of the PLL and all MRs were satisfied.

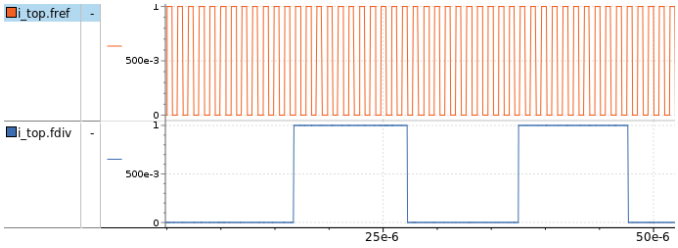

Fig. 3. PLL faulty behavior - dead zone effect revealed by MR

To summarize the experiments, the MT-based approach effectively verifies the LNA and PLL without the need of reference models.

Future work: In future, we plan to investigate the following two directions, 1) validate the MT-approach at SPICE-level, 2) check the quality of MRs.

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