# Remote Configuration Methodology for IEEE 1687 Scan Networks

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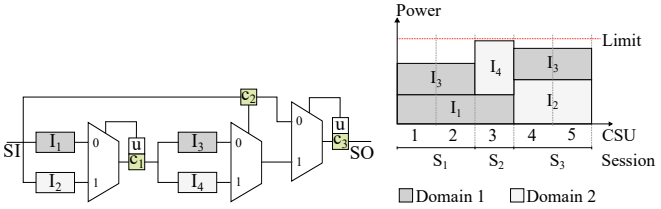
***Abstract*—The growing complexity of modern system-on-chips necessitates the incorporation of effective scan infrastructures to provide efficient access to the embedded instruments. IEEE 1687 Std. (IJTAG) addresses this fundamental requirement by introducing a flexible access methodology which contributes to the reduction of overall access time. This effectiveness is enabled by exploiting programmable elements that are configured to shorten the length of the scan chain. However, this method incurs some additional configuration overhead to the overall access time. This work tackles the problem by proposing a remote configuration approach for multi-power domain IJTAG networks based on given power and access requirements. The experimental results prove a considerable reduction of access time overhead compared to the benchmark networks.**

## I. Introduction

IEEE 1687 Std. (IJTAG) has introduced an efficient technique to cope with the challenge of long scan chains while accessing the embedded instruments in the state-of-the-art *System-On-Chips* (SoCs) [1]. Programmable elements like *ScanMux Control Bits* (SCBs) and *Scan Insertion Bits* (SIBs) enable the reconfiguration of the IJTAG scan networks to set up shorter scan chains in every access session. Since SIBs can be modeled by multiplexers, the rest of this paper focuses on multiplexer-based IJTAG networks. According to the latest chip design paradigms, SOCs can be partitioned into several power domains to better manage the workload [2]. Every domain has a power constraint that limits the number of instruments accessible over an access session concurrently. Since the test process starts after the end of the design phase, the instruments' power consumption and their required access patterns are provided as given constraints [3]. Based on this information, test schedulers are able to calculate an optimized access sequence to the instruments that minimizes the overall test time [4]–[6].

Fig. 1a shows an example of a small IJTAG network that provides access to instruments $I_1$ to $I_4$ using two inline SCBs $c_1$ and $c_3$ and the remote SCB $c_2$. Despite inline SCBs, which are placed on the same chain as the corresponding scan multiplexer, the remote SCBs control the scan multiplexer from another chain. The network of Fig. 1a allows for the creation of five different paths between $SI$ and $SO$, which yields four combinations of instruments, namely $\{(I_1, I_3), (I_1, I_4), (I_2, I_3), (I_2, I_4)\}$. Assuming $\{a_1 = 3, a_2 = 2, a_3 = 2, a_4 = 1\}$ as the required number of accesses to the instruments $i_1$ to $i_4$, Fig. 1b shows a valid access schedule




(a) (b)

Fig. 1: (a) A small IJTAG network (b) The corresponding schedule based on power constraints and access requirements

for Fig. 1a. Since the concurrent activation of $I_2$ and $I_4$ exceeds the power limit, the schedule cannot include a session containing both instruments. Every access to the instruments of the active scan chain is provided during a *Capture-Shift-Update* (CSU) cycle. A number of CSUs containing exactly the same instruments are called an access session. The schedule in Fig. 1b requires five CSUs over three sessions to fulfill all required accesses. The advantage of IJTAG over the legacy access approaches is excluding the redundant segments of the design in every session and, hence, shortening the active scan chain, which yields lower test costs. However, introducing the programmable elements itself incurs some access time overhead [7]. In an access schedule with $n_s$ CSUs and $c_s$ inline SCBs in session $s$, the overall time overhead due to inline configuration bits would be $\sum_{s \in S}(n_s \cdot c_s)$, where $S$ indicates the set of access sessions. Every access to the instruments requires two extra clock cycles to shift the data through $c_1$ and $c_3$, causing an overall time overhead of 10 clock cycles, as exemplary in Fig. 1b.

During the manufacturing test, the time spent on each fabricated circuit has a significant impact on the total cost [3]. Significant research has been carried out to reduce the overall test time in reconfigurable scan networks [8]–[12]. However, these works either are not applicable to multi-power domain networks or do not optimize the network's topology to achieve improved accessibility. This paper introduces a remote configuration methodology for controlling the multi-power domain IJTAG networks based on given power and access constraints. The proposed method significantly reduces the total access time overhead by designing a configuration network without affecting the intended accessibility of the instruments.

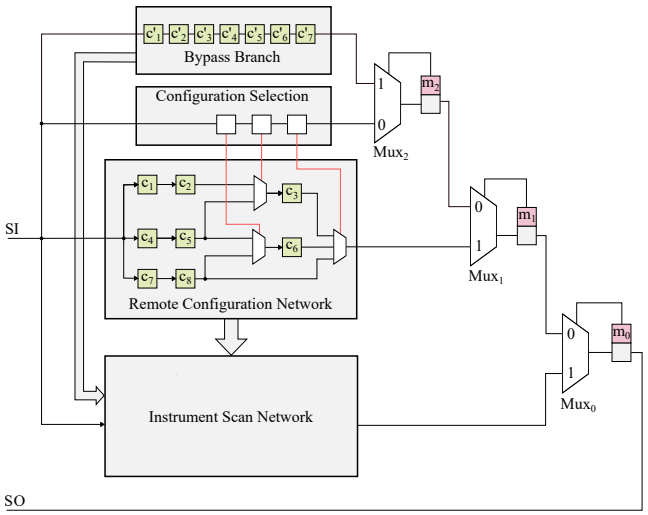



Fig. 2: proposed remote configuration architecture

## II. Proposed Configuration Methodology

The structure of an IJTAG network described by *Instrument Connectivity Language* (ICL) can be modeled as a directed acyclic graph [4], [13]. Given the power constraints and access requirements, an optimized schedule is calculated using the method introduced in [6]. The active instruments in every session of the schedule are accessed through a scan chain starting from *Scan-In* (SI) and terminating at *Scan-Out* (SO). In order to find ScanMuxes and their active inputs that contribute to the current chain, the IJTAG network is modeled as a Boolean expression in *Conjunctive Normal Form* (CNF) [5], [14]. This CNF representation defines all potential scan chains between SI and SO. In every satisfying model of this propositional formula, those literals that are assigned to $True$ indicate the active elements on the corresponding scan chain. Active ScanMuxes are extracted for every session of the schedule. The corresponding ScanMux control bits are subsequently connected to each other to form a path between SI and SO. Repeating this process for all sessions generates a directed acyclic graph of configuration elements. This incremental procedure creates a new IJTAG network that is used as a remote configuration block for controlling the instrument scan network. Since different chains potentially share the same ScanMux control bits, the synthesized configuration network graph may include merging nodes implying the creation of multiplexers. The control bits of these multiplexers are implemented serially on a remote chain called *Configuration Selection*. This prevents a time overhead while shifting the configuration vectors through the *Remote Configuration Network*. As the generated configuration network is itself an IJTAG network, it does not require a separate controller and, hence, uses the same controller as the main *Instrument Scan Network*.

Fig. 2 shows an example of the proposed remote configuration architecture. Eight hypothetical inline SCBs of the scan network are implemented as *Remote Configuration Network* with eight single-bit configuration registers and three multiplexers. The required control bits for the generated multiplexers are placed in the *Configuration Selection* block. More precisely,

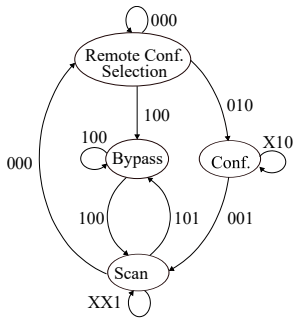



Fig. 3: Control states of proposed remote configuration architecture by considering ($m_2$, $m_1$, $m_0$) as input

the proposed method divides the IJTAG network into three main segments. The first part is *Instrument Scan Network* which contains no configuration elements and includes only the instruments and multiplexers. The scheduler calculates an optimized sequence of access to these instruments. The second segment is, in fact, another IJTAG network composed of configuration elements controlling the multiplexers of instrument scan network. Every chain of the *Remote Configuration Network* activates one chain of the *Instrument Scan Network* and establishes an access session accordingly. The last segment is a branch of solely programmable registers that select the required chain for the network's configuration. As is shown in Fig. 3, three multiplexers *Mux*$_2$, *Mux*$_1$ and *Mux*$_0$ enable the selection between three operation modes: configuration selection, remote configuration, and instrument scan. Although the proposed tailored architecture improves the feature of time overhead reduction in IJTAG networks, it limits the flexibility of the network. In order to maintain flexible access to the instruments, an additional bypass mode is provided. This flexibility enables extra configuration capabilities in case of future changes in the access plan.

At the initial state, all configuration bits are set to $0$ and, hence, the *Configuration Selection* branch is active. The first selection is made over one CSU to program the configuration network for setting up the first chain of the scan network. During the first CSU, three extra bits $(0, 1, 0)$ are appended to the data being shifted through the configuration selection branch to prepare (*Mux*$_1$, *Mux*$_0$) for the next step and, consequently, activate the *Remote Configuration Network*. After activating the configuration network, the required pattern for controlling the ScanMuxes of the *Instrument Scan Network* is shifted through the already created remote configuration chain. The mode selection bits $(0, 1)$ are appended to the configuration data. An update signal from the IJTAG controller activates the *Instrument Scan Network*, which enables the shift of instrument access data or test patterns. In this mode, only one control bit of *mux*$_0$ is appended to the scan data. Since *mux*$_1$ is already set to $0$, assigning $0$ to *mux*$_0$ at the end of every instrument access session resets the whole system to the configuration selection mode for starting the next session. The proposed method provides tailored access to the instruments according to an optimized access plan devised during the design phase. However, the proposed approach will not be optimized for other

possible access schedules. In order to add flexibility for possible future scheduling scenarios, the *Bypass Branch* can exclude the configuration and selection segments when required. This branch that can be activated by $mux_2$ is a remote chain, which includes all control bits of the *Instrument Scan Network*. This enables the concurrent activation of every combination of the intended instruments at the cost of a longer configuration chain. In fact, some control bits can be excluded from this chain according to design requirements, such as exclusive instrument access. Despite the inline SCBs, which contain two Flip-Flops, the proposed remote configuration elements are implemented by one Flip-Flop. Therefore, the proposed method does not incur considerable area overhead in comparison to the inline configuration approach.

## III. Experimental Results

In order to evaluate the efficiency of the proposed method, a framework is developed in C++. All experiments are applied to the ITC'16 IJTAG benchmark set [15] and are carried out on a machine holding AMD Ryzen 7 Pro 4750U processor and 16GB of main memory. Table I compares the obtained results with the benchmark networks. The experiments include the networks with different sizes whose names are listed under column (1). All networks are divided into three power domains. For every network, a scheduling scenario is designed by assigning random power consumption and access to the instruments. After calculating the optimized access sequence, the scan chains are extracted. Next, the overall clock cycles required to cover all instruments are calculated for both benchmark and generated networks. The results reported in columns (2) and (3) show a considerable reduction of access time overhead in the proposed networks. The number of configuration elements in the generated networks, without any bypass branch, is presented in column (5). The experimental results show an average of 70.8% reduction in the overall access time overhead in comparison to the configuration method used in the benchmark networks. The basic scheme of the proposed networks without the bypass branch requires an average of 23.7% fewer programmable elements. However, providing full flexibility for every possible access scheme by adding a bypass chain incurs an average of 24.7% extra overhead compared to the benchmark networks. Although the proposed methodology aims to reduce the overall access time, the area overhead can be reduced by omitting the bypass branch.

TABLE I: Comparing the time and area overhead of the proposed architecture with ITC'16 benchmark networks

| (1) **Network** | **Time Overhead (Clk)** | | **Area Overhead (Bits)** | |
|---|---|---|---|---|
| | (2) ITC'16 | (3) Proposed | (4) ITC'16 | (5) Proposed |
| Mingle | 418 | 199 | 26 | 25 |
| BasicSB | 412 | 130 | 20 | 19 |
| TreeFlat | 1736 | 166 | 26 | 19 |
| TrapOrFlap | 700 | 232 | 24 | 23 |
| q12710 | 3596 | 825 | 54 | 40 |
| a586710 | 2788 | 832 | 64 | 40 |
| t512505 | 38645 | 18954 | 318 | 318 |
| p22810 | 130134 | 49492 | 540 | 327 |
| p34392 | 2874 | 2929 | 194 | 105 |
| N17D3 | 3468 | 460 | 30 | 23 |
| N32D6 | 16657 | 992 | 46 | 31 |
| N73D14 | 49307 | 3014 | 92 | 69 |
| N132D4 | 91704 | 8896 | 158 | 113 |
| NE600P150 | 246283 | 46809 | 802 | 527 |
| NE1200P430 | 1980576 | 448222 | 1622 | 1248 |

## IV. Conclusion

This paper proposed a novel methodology to synthesize a remote configuration circuit for multi-power domain IJTAG networks. According to the results, the presented method contributes to the reduction of test costs by enabling shorter overall instrument access time. In the end, the experiments prove the scalability of the proposed approach.

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